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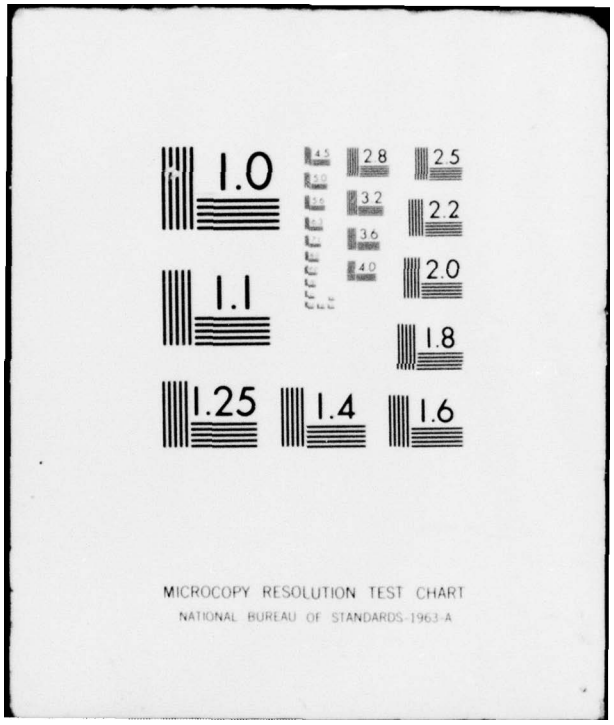
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A monolithic surface wave transversal filter was designed, fabricated, and evaluated. The semiconductor and acoustic elements were developed on (001) p-type silicon oriented for acoustic transmission along the (100) direction. Surface acoustic waves were generated by zinc oxide film layer transducers into an array of 31 metal-gate NMOS piezoresistive FET taps. The drain lines of all taps were connected to serve as the rf output. The phase and amplitude of each tap was controlled by information read into a digital static shift register and a bucket brigade device respectively. The die size for a single 31 bit filter

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was .810 inch by .160 inch.

The conversion loss of the 9.5 finger pair zinc oxide film layer transducers was 15 dB. The piezoresistive tap coupling efficiency was in the 35 to 40 dB region under normal operating conditions. The overall device efficiency in developing a spread waveform from a short (100 ns) rf input pulse was 75 dB which include losses due to signal expansion, channel division, matching and parasitics. The direct coupled signal level was 90 dB below the input signal level and the signal to noise ratio of the spread pulse was approximately 20 dB. The bucket brigade device was effective in controlling tap amplitude over a 10 dB range and the digital shift register provided for random biphase coding of the taps. The yield of working transversal filter chips was greater than 40 percent from 3 inch silicon wafers.

There were problems which prevented a full-scale evaluation of the correlation properties of the device. Acoustic reflections from the MOSFET detector taps caused a 10 dB degradation in the spread waveform. Phase coding individual taps also caused some signal amplitude degradation.

The development represented an important step toward the realization of a compact, low cost highly versatile matched filter device for signal processing applications in communications equipment. It permitted a quantitative assessment of various aspects of ZnO/Si-MOSFET technology and demonstrated the viability of the monolithic integration of SAW and semiconductor circuitry on silicon.

PREFACE

This report was prepared by the Government Electronics Division of Motorola Inc. under Air Force Contract F30602-76-C-0134. The work was administered by the Rome Air Development Center, Griffiss AFB, New York. Henry J. Bush was the technical program monitor for RADC.

Technical work on the program began 22 March 1976 and was completed 22 July 1977. The project was a cooperative effort involving various groups and facilities at the Government Electronic Division (GED) and Semiconductor Group (SG) of Motorola Inc. Fred Hickernell of the Integrated Circuit Facility (ICF) of GED was the project leader. Dan Ong of the Motorola Integrated Circuits Applications Research Laboratory (MICARL) coordinated the SG efforts. Major device design and layout work was done by Don Olson of GED. Mask generation, material growth and wafer preparation, wafer processing, test and slicing was the responsibility of SG. Transducer design and fabrication, logic and rf system design and fabrication, packaging and final rf testing was the responsibility of GED. Larry Flaherty (GED) was the Program Manager.

The following individuals made significant technical contributions to the program: Don Forbes (SG), wafer fabrication; Ron Hayman and Ellie Mason (MICARL), mask layout; Ken Pindur (SG), mask fabrication; Dick Yanez (MICARL), process development and coordination, Oscar Santa Cruz and John McDonald (MICARL), wafer processing; Bob Collins and Jim Ward (MICARL), wafer electrical evaluation; Fred Hickernell (GED), ZnO transducer fabrication; Don Olson and Jim Hinsdale (GED), test circuitry; Ron Rose (GED), test circuit fabrication; Mike Adamo (GED), device packaging and final rf test; Ron Lawson (MICARL), device analysis; and Dave Leeson and Al Kapanicas (GED), assembly and rf test.

The final report was prepared by Fred Hickernell, Don Olson and Mike Adamo.

EVALUATION

This report describes developments which have served to demonstrate the inability of the monolithic integration of SAW and semiconductor elements and permitted an assessment of various aspects of the technology. The capability for simultaneous, real-time tap phase and amplitude control provides implementations of real-time adaptive signal processing techniques. Considering the amount of signal processing that can be done in such a small form factor at low cost, application of the monolithic technology is quite attractive. However, as noted in the report, certain areas need additional work to realize the full potential of the technology.

Henry J. Bush

HENRY J. BUSH
Project Engineer

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INTRODUCTION

1. MONOLITHIC PROGRAMMABLE MATCHED FILTER CONCEPT

There is an increasing need for acoustic components to be used in microwave communications and radar systems which acquire and process large amounts of signal data. These acoustic components require a wide bandwidth capability, a long storage or delay time, and a built-in filter or coding function. A substantial number of current requirements for signal processing systems can be met using tapped surface acoustic wave devices. Such devices can simplify processing circuitry and represent a reliable, low cost alternative to present electronic techniques.

Surface wave devices are being used to perform matched filter functions in communications and radar systems where it is desirable to unambiguously transmit data in the presence of noise and/or jamming signals. There have been three levels of development. First there are fixed coded devices, where a series of phased interdigital metallic electrodes are implemented on a piezoelectric substrate and packaged as a discrete component. Electronic switching and logic functions in lumped circuit and hybrid form have been incorporated with the fixed coded devices to develop a second level of surface wave encoders and decoders which are programmable. While integrated circuits can be used in such hybrid configurations, the separate manufacture and interconnection of acoustic and electronic devices creates cost inefficiencies and reliability problems due to circuit complexity. Because the development trend in signal processing subsystems is toward a higher degree of component integration in a miniaturized form factor and ultimately requires production in substantial quantities, monolithic building blocks combining the acoustic encoding and decoding functions with electronic functions such as switching, mixing and amplification on a single substrate should lead to considerable cost savings, improved reliability and size reduction. It is this third level of development, the monolithic programmable matched filter device, which will provide the greatest opportunities and challenges for the future.

Silicon provides an excellent base material for the development of a monolithic programmable matched filter. Rayleigh waves can be efficiently generated on its surface using piezoelectric film layer transducers. MOSFETs provide a convenient means for broadband detection of the surface waves through the piezoresistive effect. The output signal level can be controlled through gate voltage bias. The piezoresistive tap can be addressed through control circuitry for arbitrary phase selection and amplitude level. Silicon also provides the basis for the integration of other semiconductor circuit elements.

A conceptual representation of the three main functional parts of a silicon based monolithic programmable device is shown in Figure 1. The various acoustic and electronic functions are developed on a properly oriented and doped silicon substrate using semiconductor process compatible-fabrication techniques. At each end of the device is a film layer transducer composed of a thin aluminum interdigital electrode structure with an overlay of piezoelectrically active sputtered zinc oxide. The transducers are the electrical inputs for rf pulses in the encoding mode and the rf bi-phase sequences in the decoding mode.

Between the two transducers is the MOSFET device taps which serve as the piezoresistive detectors of the surface acoustic wave energy generated by the transducers. These MOSFET cells are placed in geometric arrangements corresponding to the desired phase coding. Binary and quad-raphase coding can be easily implemented. The device output is taken from the parallel connected drain lines of the MOSFET device taps.

The third major feature is the semiconductor circuitry controlling the phase and amplitude of the MOSFET detector taps. The information in this control circuitry may be statically or dynamically programmed. It codes and weights the taps according to the desired signal processing function.

For certain analog signal processing functions, there will be performance, size and economic advantages favoring the monolithic integration of surface acoustic wave and semiconductor device functions on a single silicon substrate. It is important to develop design capabilities, and improved material properties and fabrication processes which permit such signal processing modules to be developed.

There have been two developments to date based on the concepts just described. The first was a 15 bit quadraphase programmable correlator operating at 60 MHz with a 10 MHz bandwidth and a 1.5 μs expanded pulse. External logic control circuitry was required. The results of this work has been described in two publications.[1,2]

The second development was the 31 bit bi-phase matched filter which preceded the present work.[3,4,5] A summary of this work follows.

2. PREVIOUS PROGRAM DEVELOPMENTS

Under a previous RADC Air Force Contract (F30602-74-C-0021) a silicon based monolithic programmable surface wave matched filter was designed, fabricated and evaluated having a ROM controlled 31-bit Si-MOSFET bi-phase tap structure. Individual matched filter devices were capable of generating and correlating 31-bit PN sequences at a carrier frequency of 100 MHz with a 10 megabit/second rate. Two of the devices were incorporated in an encoder system with controlling logic circuitry which permitted contiguous signal generation by random selection of codes from the 6 x 31 bit read only memory on the device. A single device was used to correlate coded signals produced by both a similar matched filter and a digitally generated signal. The device provided a high degree of signal processing system integration on a single silicon substrate.

Figure 2 shows the device developed. The device was fabricated on the (110) surface of a 2.5-3.0 ohm-cm, n-type silicon substrate having a thickness of 0.020 inch. The overall device size was 770 x 75 mils. A piezoelectric film layer transducer was formed at each end of the MOSFET array using a 12 μm sputtered film of ZnO overlying a 10 finger pair interdigitated aluminum film structure on oxidized silicon. One transducer was used when the device was operated in the encode mode and the other was used for decoding. A ground shield was placed between the transducers and the MOSFET tap structure to minimize direct signal coupling. The direction of acoustic wave propagation of the transducers was aligned to the [110] direction of the silicon substrate to achieve strong piezoresistive coupling to the MOSFET detectors.

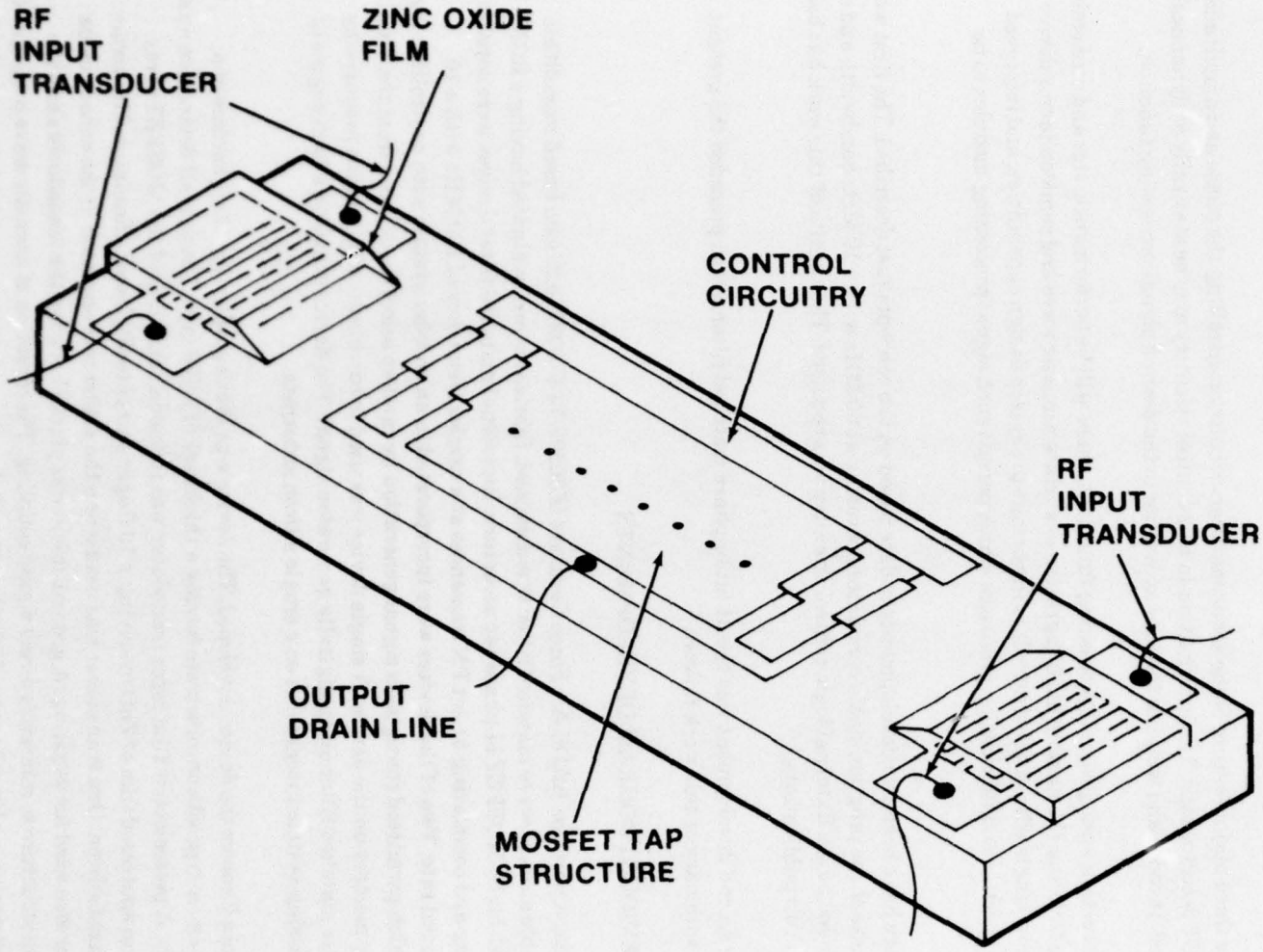


Figure 1. Monolithic ZnO/Si-MOSFET Programmable Surface Acoustic Wave Matched Filter

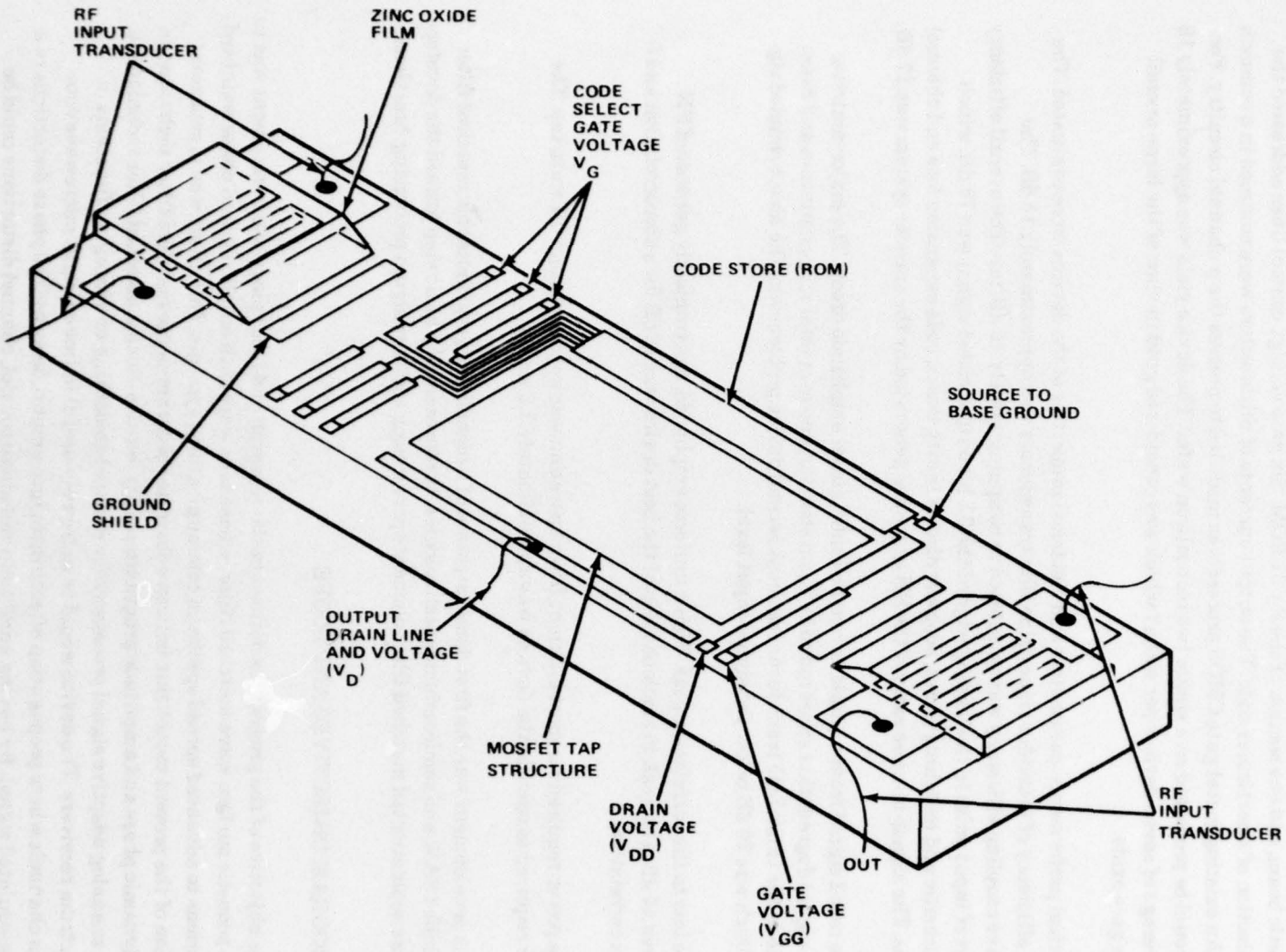


Figure 2. Monolithic ZnO/Si-MOSFET ROM Programmable Surface Acoustic Wave Matched Filter

A series of 31 MOSFET cells were placed between the two transducers. Each cell contained two MOSFET detectors (W = 20 mil, L ≅ 0.2 mil) having channels displaced by ½ wavelength normal to the acoustic beam, and one section of the 6 x 31 ROM. Six gate voltage control lines addressed the ROM for selection of a particular code. The output currents of all detectors were summed in a common drain line. An existing metal gate CMOS process was modified to process the p-channel circuitry. Forty devices could be processed on a single two inch silicon wafer. The device yield was approximately 18 percent (average of seven devices per wafer) which was considered good in view of the large overall area of thin gate oxide.

Critical performance parameters and electrical properties of the devices were evaluated. The conversion efficiency of individual zinc oxide film transducers was approximately 15 dB. The piezoresistive coupling efficiency was calculated to be approximately 40 dB/tap. The overall efficiency from a short rf input pulse to the leading edge of the 31-bit output coded signal was 78 dB, which included parasitic and matching losses, acoustic discontinuity losses, code expansion loss and channel division loss. The signal-to-noise ratio of the PN sequence generated by the encoder system was 17 dB.

The coded signal from a single device had substantial amplitude droop. The major contributors to this signal degradation appeared to be beam steering due to crystal misorientation and beam rotation due to the thick ZnO transducer region. A second device problem was the direct coupled signal level, which was 70 dB below the signal input level.

The loss to the correlation peak from a uniform amplitude, electronically generated PN sequence was 44 dB. The peak to sidelobe ratio of the best device was 12 dB for autocorrelation and 8 dB for cross correlation.

The power required for most efficient filter operation was approximately 0.1 watt/tap. The total power required to operate the devices was approximately 3.2 watts.

This development was the first demonstration of a monolithic programmable matched filter which combined SAW and semiconductor technologies. It represented a basic step toward the development of more sophisticated matched filter elements performing complex signal processing functions.

3. PROGRAM OBJECTIVES AND SCOPE

The objective of the program as defined in the research and technology work statement was to develop an acoustic surface wave matched filter, whose taps were both amplitude and phase weighted, for applications to advanced spread spectrum communications systems. This effort was to represent an expansion of the present monolithic (silicon substrate) programmable matched filter technique to include a dynamic phase and amplitude programmability feature. Such a matched filter technique is applicable to analog adaptive signal processors for channel smoothing or averaging functions in spread spectrum receivers. The device would be extremely useful in line-of-sight microwave communication channels where propagation effects introduce amplitude as well as phase distortions to a PN phase modulated signal. By having amplitude and phase control, channel distortions could be minimized to enhance signal-to-noise ratio.

The main thrust of the effort was to derive a realistically producible transversal filter which provided analog tap amplitude weighting of a programmable phase coded surface wave multiple tap delay line. The device was to be developed from a combination of metal-oxide-semiconductor (MOS) and surface acoustic wave (SAW) technologies to achieve a cost, size and weight effective implementation which is amenable to LSI mass production processes. The scope of the effort included study, design fabrication, evaluation and a breadboard model feasibility demonstration.

The scope of the effort was limited to developing the mechanism(s) for controlling the tap phase and amplitude in response to externally supplied control signals. The effort was limited to matched filter functions. The sequence generation necessary for demonstrating the perfomance of the matched filter was to be provided by either a digital or surface wave technique.

The basic device to be utilized in the effort was the monolithic programmable matched filter built under Contract F30602-74-C-0021. All design modifications necessary for achievement of both phase and amplitude weighting were allowed. It was also within the scope of the effort to alleviate the problems of amplitude droop and direct rf feedthrough, as encountered in the previous contract. It was desired to maintain, as much as possible, the integrity of the technology developed under the previous contract. Therefore, the circuit design developed under this new effort should integrate into the matched filter structure, in LSI form, as many of the new functions as possible. Toward this end, however, it was realized that the complexity and size of the resultant circuit could drive the yield toward zero. A judicious compromise of on-substrate to off-substrate functions would have to be made to achieve a realistically producible device.

The surface wave transversal filter was to have the following basic characteristics.

Operating Frequency	100 MHz
Bandwidth (3dB)	10 MHz
Tap Spacing	100 ns
Code Type	Bi-Phase Modulation
Programmability Features	Tap Phase and Amplitude

The tap amplitude control was to be analog with a goal of 20 dB.

Operational factors to be evaluated included conversion efficiency of the input transducers and the output taps, code switching speed, correlation properties, range and speed of tap output amplitude control, consumed dc power and signal to noise. Design consideration was to be given to trade-offs with production viability and cost, and partitioning of functions on/off the substrate versus cost. Special attention was to be given to minimizing direct rf feedthrough and amplitude droop.

4. PROGRAM SUMMARY

The monolithic surface wave transversal filter designed, fabricated and evaluated under this program had the basic features shown in Figure 3. The semiconductor and acoustic elements were

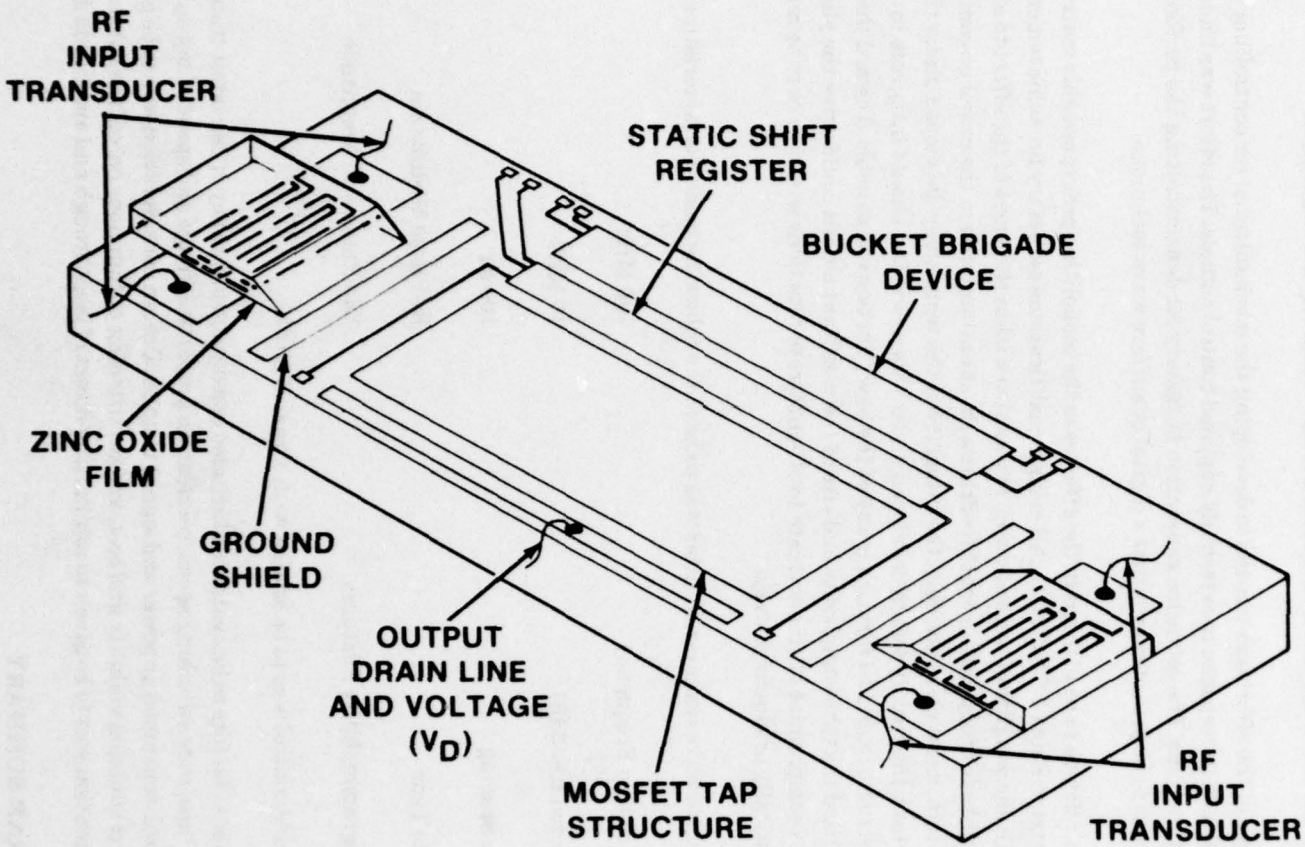


Figure 3. Monolithic Surface Wave Transversal Filter

developed on (001) p-type silicon oriented for acoustic transmission along the [100] direction. Surface acoustic waves were generated by zinc oxide film layer transducers into an array of 31 metal-gate NMOS piezoresistive FET taps. The drain lines of all taps were connected to serve as the rf output. The phase and amplitude of each tap was controlled by information read into a digital static shift register and a bucket brigade device respectively. The die size for a single 31 bit filter was .810 inch by .160 inch.

The design of semiconductor and acoustic elements was facilitated by computer programs used to specify parameters and analyze circuit configurations. Computer aided techniques were used for circuit layout and development of the processing masks. A total of 48 patterns were used to compose the required mask set.

Two lots of ten 3 inch wafers were ultimately processed using a modified CMOS process to obtain working devices. The semiconductor circuits were fabricated first followed by the acoustic film layer transducers. Some difficulty was experienced in obtaining the proper implant level for semiconductor devices. It was necessary to go through three processing cycles to obtain the required performance. There were 37 devices on a single 3 inch wafer.

The conversion loss of the 9.5 finger pair zinc oxide film layer transducers was 15 dB. The piezoresistive tap coupling efficiency was in the 35 to 40 dB region under normal operating conditions. The overall device efficiency in developing a spread waveform from a short (100 ns) rf input pulse was 75 dB which include losses due to signal expansion, channel division, matching and parasitics. The direct coupled signal level was 90 dB below the input signal level and the signal to noise ratio of the spread pulse was approximately 20 dB. The bucket brigade device was effective in controlling tap amplitude over a 10 dB range and the digital shift register provided for random biphase coding of the taps.

There were problems which prevented a full-scale evaluation of the correlation properties of the device. Acoustic reflections from the MOSFET detector taps caused a 10 dB degradation in the spread waveform. Phase coding individual taps also caused some signal amplitude degradation.

The yield of good transversal filter chips was in the 40 to 50% range. It appears that this type of transversal filter technology can be implemented with good performance characteristics and be mass producible at low cost.

SECTION II

DESIGN

1. BASIC DESIGN RELATIONSHIPS

The monolithic surface wave transversal filter required design in three functional areas; 1) film layer transducer, 2) piezoresistive taps, and 3) control circuitry. In this subsection those basic design relationships which characterize the performance of each of these functional areas will be considered. The specific designs used are described later in this section.

a. Piezoelectric Film Layer Transducer

Silicon is a nonpiezoelectric semiconductor. This precludes the direct excitation of surface elastic waves on silicon using an electro-acoustic conversion process. Attempts have been made to generate elastic waves in silicon through the piezoresistive effect but such experiments have been unsuccessful. The most efficient and process compatible method of surface wave excitation is the piezoelectric film transducer. This technique is characterized by the deposition of a piezoelectrically active film on the substrate with an interdigital electrode placed at either the upper or lower boundary of the film.

A variety of piezoelectric film materials could be considered as the transducing media. Based upon high coupling efficiency, ease of fabrication, and proven performance, sputtered zinc oxide films are considered the best. The design parameters which are characteristic of piezoelectric film layer transducers are considered with zinc oxide as the film layer. The ability of zinc oxide sputtered films to efficiently excite surface acoustic waves on fused quartz and oxidized silicon has been demonstrated.[6,7]

In order to properly design the correct interdigital electrode finger spacing corresponding to acoustic wave generation at a specified frequency, it is necessary to determine the surface acoustic wave velocity of the layered media. In principle this can be accomplished by setting up the wave equations and boundary conditions and using computer iteration techniques involving complex functions to realize a numerical velocity value. This velocity value is a function of the elastic dielectric and piezoelectric parameters of substrate and layer(s) and depends upon the thickness of the layers. Because normally only bulk parameters are known, in practice it is necessary to refine the velocity value by experimental measurement.

To illustrate this effect, Figure 4 shows the theoretical and experimental velocity characteristic of a zinc oxide film layer on fused quartz. For very thin film layers, with thickness to wavelength ratios (h/λ) less than 0.1 there is less than a 1% deviation. For h/λ near one, the propagation velocity is characteristic of the zinc oxide film layer, and the deviation is approximately 5%, clearly indicating a substantial difference between thin film and bulk crystal values.

For the silicon based transversal filter it will be necessary to consider oxide layers between the silicon and the zinc oxide film layer. These oxide layers consist of thermally grown SiO_2 and

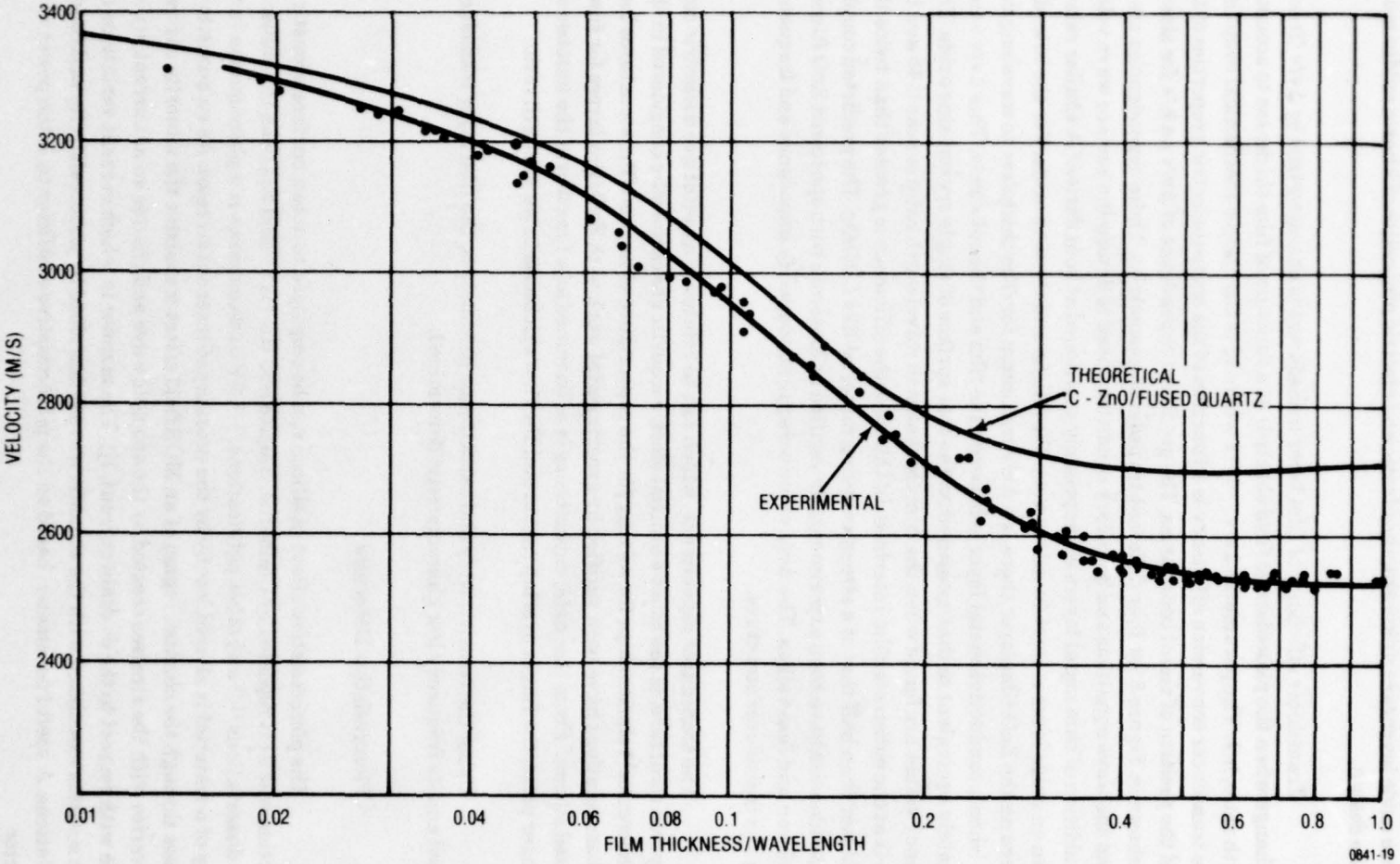


Figure 4. Velocity characteristic for Zinc Oxide Film Layer on Fused Quartz

deposited doped glasses necessary for the formation of the MOSFET devices. Since the elastic properties of these oxide layers are unknown, the elastic and electric properties of known oxides must be used for the design.

Transducer efficiency of film layer transducers is characterized by $\Delta v/v$ (fractional velocity change when the piezoelectric field shorted) as a function of film thickness to acoustic wavelength ratio, h/λ. The parameter $\Delta v/v \simeq k^2/2$ where k^2 is the electro-mechanical coupling constant. The transducer conversion efficiency is a function of the acoustoelectric properties of the film layers and the position of metal boundaries. The predicted dependence of $\Delta v/v$ on h/λ for zinc oxide on silicon is shown in Figure 5 for four different transducer geometries. These dependencies are determined from the wave equations and boundary conditions used to determine surface wave velocity with the addition of thin metal layers appropriately positioned at boundaries.[8] A similar relationship holds when an oxide layer is introduced between the silicon and the zinc oxide. For the interdigital (ID) pattern on the ZnO film layer there is a $\Delta v/v$ maximum for film thickness to wavelength ratios near 0.05 when a conductive metal layer is between the film and the substrate. This $\Delta v/v$ value is approximately equivalent to that measured on the free surface of single crystal zinc oxide. The highest efficiency values are found when the film thickness to wavelength ratio is near 0.45 and the ID structure is at the substrate/film interface. In this case the efficiency is greater than twice that of ZnO and better than half that of a strong coupling material like $LiNbO_3$. The predicted coupling efficiency dependencies have been experimentally verified at Motorola with sputtered ZnO films on oxidized silicon and fused silica. The $\Delta v/v$ value is required to specify impedance and frequency-loss values for the transducer structure.

The transducer capacitance, which can be related to an effective dielectric constant for the layered structure, is the other essential electroacoustic characteristic considered in the design. Theoretical relationships for solving for the capacitance of layered film structures have been given.[8] These relations have been verified by experimental work with ZnO film layers for fused silica and oxidized silicon.[7] From this data, capacitance is determined as a function of the number of interdigital finger pairs, the finger overlap region and the film thickness to wavelength ratio.

Using the velocity, $\Delta v/v$ and capacitance parameters, the film layer transducer may be designed and its frequency loss characteristic determined.

b. Piezoresistive Detectors

The piezoresistive effect in silicon can be employed to detect surface acoustic waves. The detection was first reported by Claiborne, Staples and Harris [9,10] and has been the subject of at least two dissertations [11,12] and other publications.[13,14,15] Piezoresistance is a phenomenon in which the resistivity of a material is altered locally by the presence of internal stresses. As an acoustic surface wave passes through the channel region of an MOS field effect transistor the minority carrier mobility varies with the stresses created by the acoustic wave and creates an ac current, i_D, small in amplitude with respect to the dc drain current, I_D. The manner in which current variations are related to stresses associated with the acoustic wave is described by piezoresistivity and conductivity tensor relations. A useful parameter, based on the piezoresistive coefficients, is the power normalized gauge factor

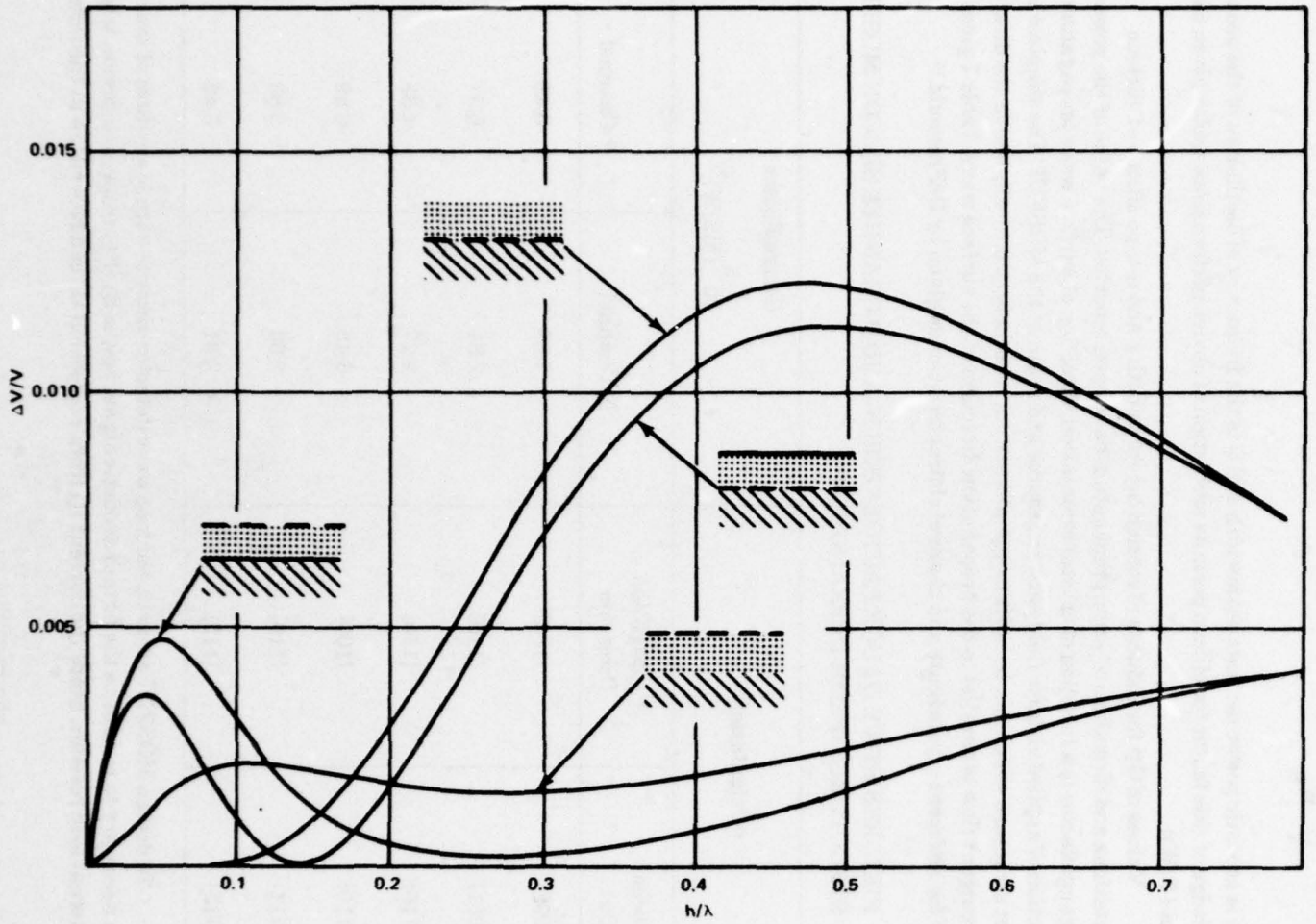


Figure 5. Coupling Efficiency Parameter Δv/v as a Function of Film Thickness to Acoustic Wavelength Ratio for Zinc Oxide on Silicon

$$G_P = \frac{\frac{i_D}{I_D}}{\sqrt{\frac{P\omega}{W_B}}} \qquad (1)$$

where P/W_B is acoustic power per unit beamwidth and ω is the frequency of oscillation of the acoustic wave. Knowledge of this factor for silicon permits prediction of device performance under given conditions of I_D and P/W_B.

Values of GP for induced inversion layers in both p and n-type silicon of various crystal orientations and directions of wave propagation have been reported. The value of the power normalized gauge factor is a function of crystal orientation, direction of surface wave propagation and the direction of applied electric field between source and drain of the MOSFET. The simplest and most compact structure which can be built using microcircuit technology is one in which the direction of MOSFET current flow is parallel to the propagation direction of the surface wave. Table 1 gives values of GP for different crystal cuts and channel characteristics as given by DeFranould.[15]

TABLE 1. PIEZORESISTIVE GAUGE FACTORS FOR N-AND P-CHANNEL SILICON MOSFET STRUCTURES (FROM DEFRANOULD[15])

Orientation		Gauge Factor $10^{-8}(MS/W)^{1/2}$	
Silicon Cut	Propagation Direction	N-Channel	P-Channel
(001)	[100]	7.08	0.46
(001)	[110]	2.81	6.31
(110)	[110]	2.27	4.36
(110)	[100]	6.45	0.80
(111)	[110]	2.63	3.83
(111)	[112]	2.31	3.42

To design MOSFET acoustic surface wave detector circuits with low values of insertion loss it is necessary to maximize the output acoustic signal power $i_D^2 R_L$, from each device, where R_L is the external load resistor. Since the current i_D from expression (1) can be written in the form,

$$i_D = I_D G_P \sqrt{P\omega/W_B} \qquad (2)$$

minimum loss for a given frequency of operation requires selection of a MOSFET substrate material with high G_P, maximizing the acoustic power per unit width induced on the silicon surface, operating the MOSFET'S at high values of quiescent drain current, and using a high value of load impedance.

The power ratio for a single MOSFET tap under the idealized conditions where 1) the MOSFET tap capacitance including parasitics has been parallel resonated, 2) the output load matches the internal load and 3) there are no parasitic resistive losses is

$$\frac{P_o}{P_i} = \frac{I_D^2 G_P^2}{4 W_B g} , \tag{3}$$

where g, the finite channel conductance, reduces the value of i_D received by the output load.

Since a surface matched filter requires the use of a series of MOSFET taps, the power delivered to the load is reduced or increased by N, the number of taps, depending upon whether it is operated in the encoding or decoding mode.

$$\frac{P_o}{P_i} = \frac{I_D^2 G_P^2 \omega}{4 W_B N g} \quad \text{(encoding)} \tag{4}$$

$$\frac{P_o}{P_i} = \frac{N I_D^2 G_P^2 \omega}{4 W_B g} \quad \text{(decoding)} \tag{5}$$

The encode and decode conditions differ in value by N^2. For example, in a 31-bit correlator there would be a 15 dB improvement under decode conditions over the loss for a single MOSFET tap and a 15 dB increase in loss for the encode condition.

For a given gate to source operating voltage, V_{GS}, it is desirable to operate in the saturation region to minimize g. To first order, the nonzero slope of the saturation region is due to a channel shortening effect. It occurs just after the device enters the saturation region when the channel length, L, becomes shortened by the depletion region of the drain-substrate junction extending into the channel. This gives rise to the approximate expression.

$$g = -\frac{I_D}{L} \frac{dL}{dV'_{DS}} \qquad [V'_{DS} = V_{DS} - V_{DS\,(sat)}] \tag{6}$$

Where V_{DS} (sat) is the drain-source saturation voltage. The value of g is a positive value since dL/dV_{DS} is a negative term. Conductance increases with I_D and is inversely proportional to L. The dL/dV_{DS} depletion term will be larger for lower values of N_D (substrate doping level).

In the analysis of the effect of MOSFET device parameters on P_o/P_i it is convenient to use the expression for the quiescent operating current in the saturation region which is given approximately by

$$I_D = 1/2 \frac{W}{L} \mu C_o (V_{GS} - V_T)^2 \tag{7}$$

where W and L are the actual channel width and length,

μ is carrier surface mobility,
C_o is oxide capacitance per unit area,
V_{GS} is gate to source voltage, and
V_T is threshold voltage.

Inserting equations (6) and (7) into equation (3) gives the following expression for the power ratio.

$$\frac{P_o}{P_i} \cong \frac{\mu C_o (V_{GS} - V_T)^2 G_P^2 \omega}{8 \left| \frac{dL}{dV'_{DS}} \right| \left(\frac{W_B}{W} \right)} \tag{8}$$

Equation (8) indicates independence of P_o/P_i on the W/L ratio of the MOSFET detector. It does indicate that the power ratio is enhanced by a high mobility and low threshold device.

Another useful relationship in detector design is the device cutoff frequency, f_c, given by

$$f_c = \frac{\mu (V_{GS} - V_T)}{2 \pi L^2}. \tag{9}$$

The cutoff frequency increases with mobility, bias voltage and decreasing channel length.

Another limitation on the design of the detector array is the need for resonating the device parasitic capacitance and matching internal impedance for optimum signal transfer. The Q of the loaded circuit, Q_L, must be less than $f_o/\Delta f = 100\ MHz/10MHz = 10$. Q_L is given by

$$Q_L = \frac{\omega_o C_{PAR}}{2 Ng} \leq 10 \tag{10}$$

where C_{PAR} is the total drain parasitic capacitance and N is the number of MOSFET taps. C_{PAR} consists primarily of drain to substrate junction capacitance, C_{DB}, drain to gate overlap capacitance, C_{GD}, both associated with the drain junctions of MOSFET detectors, and C_{DL}, the capacitance of the drain current summing line. Although equation (4) indicates the desirability of low g values, equation (10) says that g must be sufficiently large to keep Q_L less than 10 for a given C_{PAR}.

The positioning of the piezoresistive taps along the propagation path requires an analysis of the propagation velocity on a medium consisting of silicon, oxides and aluminum. This is difficult to handle theoretically but an estimate is required. The oxide layers will reduce the Rayleigh velocity by 3-5% for film thickness to wavelength ratios near .05. By using known elastic constants of glass layers a velocity can be calculated.

c. Control Circuitry

The circuitry controlling the MOSFET taps was to be capable of arbitrarily selecting the bi-phase code and weighting the output amplitude from each tap. To do this a digital static shift register, (DSSR) and bucket brigade device (BBD) were proposed for development. A digital static shift register was chosen because of its ability to establish the required code by a serial input and store it without sacrifice in speed of operation, which is BBD controlled. The bucket brigade represented a serial input device for short term storage of the tap amplitude information.

In order to achieve the required 20 dB tap amplitude range, it is necessary that the ratio of maximum detector dc drain saturation current to minimum detector dc drain saturation current $I_{D\,MAX}/I_{D\,MIN} \geq 10$. The MOSFET maximum and minimum gate voltages $V_{G,MAX}$ and $V_{G,MIN}$ required to achieve this current range should obey the relationship:

$$\frac{\left|V_{G,\,MAX} - V_T\right|}{\left|V_{G,\,MIN} - V_T\right|} \geq \sqrt{10} \tag{11}$$

where V_T is the MOSFET detector threshold voltage.

Both DSSR and BBD devices can be implemented using MOSFET technology. Their design was to be based on theoretical design guidelines and experimental work with similar devices.

2. MATERIAL AND PROCESS SELECTION CRITERIA

The type and orientation of the silicon and selection of the MOSFET process is governed primarily by the semiconductor circuit elements and secondarily from acoustic considerations. The efficiency of surface wave generation by the film layer transducer is essentially independent of crystal orientation and doping level. The surface wave velocity characteristic is important, however, since for certain propagation directions on silicon, deep lying pseudo-waves satisfy the boundary conditions. In particular the (001) [110] silicon configuration has such a velocity condition and was not considered.

From the viewpoint of MOSFET detector efficiency, PMOS and NMOS technology can be compared using equation (8). If it is assumed that structural properties are similar, the power ratio for NMOS to PMOS becomes

$$\frac{P_N}{P_P} = \frac{\mu_N \left(V_{GS} - V_T\right)_N^2 \; G_{PN}^2}{\mu_P \left(V_{GS} - V_T\right)_P^2 \; G_{PP}^2} \cdot \frac{\left|\frac{dL}{dV'_{DS}}\right|_P}{\left|\frac{dL}{dV'_{DS}}\right|_N} \tag{12}$$

The mobility of N-channel exceeds that of P-channel by a factor of 2.5. Assuming equal V_{GS}, the V_{GS}-V_T value for N-channel will be slightly larger due to a lower threshold voltage. The gauge factor ratio can be higher for N-channel depending upon the cut as seen in Table 1. However, it has been noted by DeFranould[15] that for N-channel devices the gauge factor decreases with increasing gate

voltage and therefore there is not a substantial difference between the higher NMOS and PMOS gauge factor cuts. The channel shortening effect is less pronounced in N-channel devices and can lead to an improvement by a factor of two. A conservative estimate is that an improvement in power output of approximately 6 could be realized by using N-channel MOSFETS. This represents an expected 8 dB improvement in detector loss. Using NMOS technology there is the capability for higher speed of operation and lower power.

Based upon these considerations it was decided to use a metal gate NMOS process and select (001) silicon with acoustic propagation and channel orientation along the [100] direction. The selection of the substrate doping level, the channel doping level and oxide thicknesses represent tradeoffs between the various parameters affecting device performance. For example, increasing the substrate doping level lowers the channel conductance value but raises the value of parasitic capacitance. It was necessary to compromise on material properties in order to realize the most efficient device.

3. ZINC OXIDE FILM LAYER TRANSDUCERS

The zinc oxide film layer transducer configuration selected was that with the interdigital electrode at the zinc oxide-silicon dioxide boundary and a floating metal plane on top of the zinc oxide. (See Figure 6) Operation was to be at the lower maximum ($\sim 0.05\lambda$) film thickness region. This choice was based upon achieving a zinc oxide film quality consistent with the 10 MHz bandwidth requirement and having good conversion efficiency. The thin film geometry also minimizes the topography of the transition between transducer film and detector region and the beam steering effects taking place in this transition region. Ease of fabrication was also a consideration.

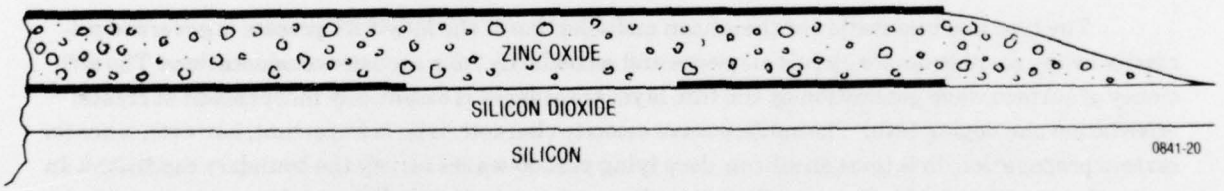


Figure 6. Zinc Oxide Film Layer Transducer Structure

Figures 7 and 8 show the velocity dispersion and coupling factor curves for a $ZnO/SiO_2/Si$ layered structure with a 57% to 43% ratio of zinc oxide to silicon dioxide. The acoustoelectric constants for (001) [100] silicon, fused quartz and C-axis normal zinc oxide were used in the calculation.[16] Metallized and unmetallized boundary conditions were applied. The curves were plotted for small thickness to wavelength ratios with Hk values from 0 to 1.0 where H is total film thickness and $k = 2\pi/\lambda$. From these relationships the point of maximum coupling factor is determined and a velocity may be specified for calculating the periodicity of the interdigital electrode.

With a velocity of 4425 m/s, the wavelength for a 100 MHz frequency is 44.25 μm or approximately 1.74 mils. A split electrode configuration was chosen with individual finger widths and spacings at $\lambda/8$ or approximately 0.218 mils. The number of finger pairs was 9.5 consistent with the required 10 MHz bandwidth. There were a total of 38 individual electrode fingers. The active finger overlap dimension was 50 mils consistent with maintaining an acoustic wave field which was slightly larger than the MOSFET taps.

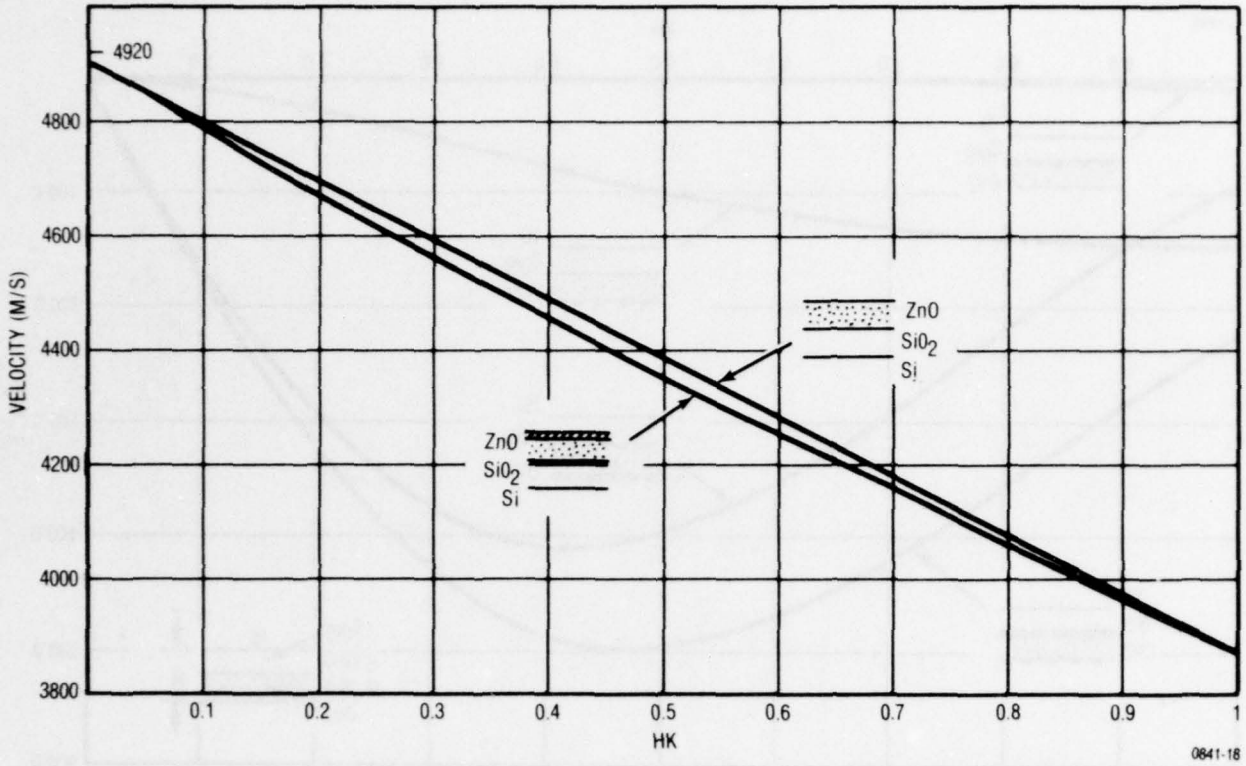


Figure 7. Rayleigh Velocity for C-ZnO/SiO_2/Si (001) [100] As a Function of Film Thickness-Wavenumber

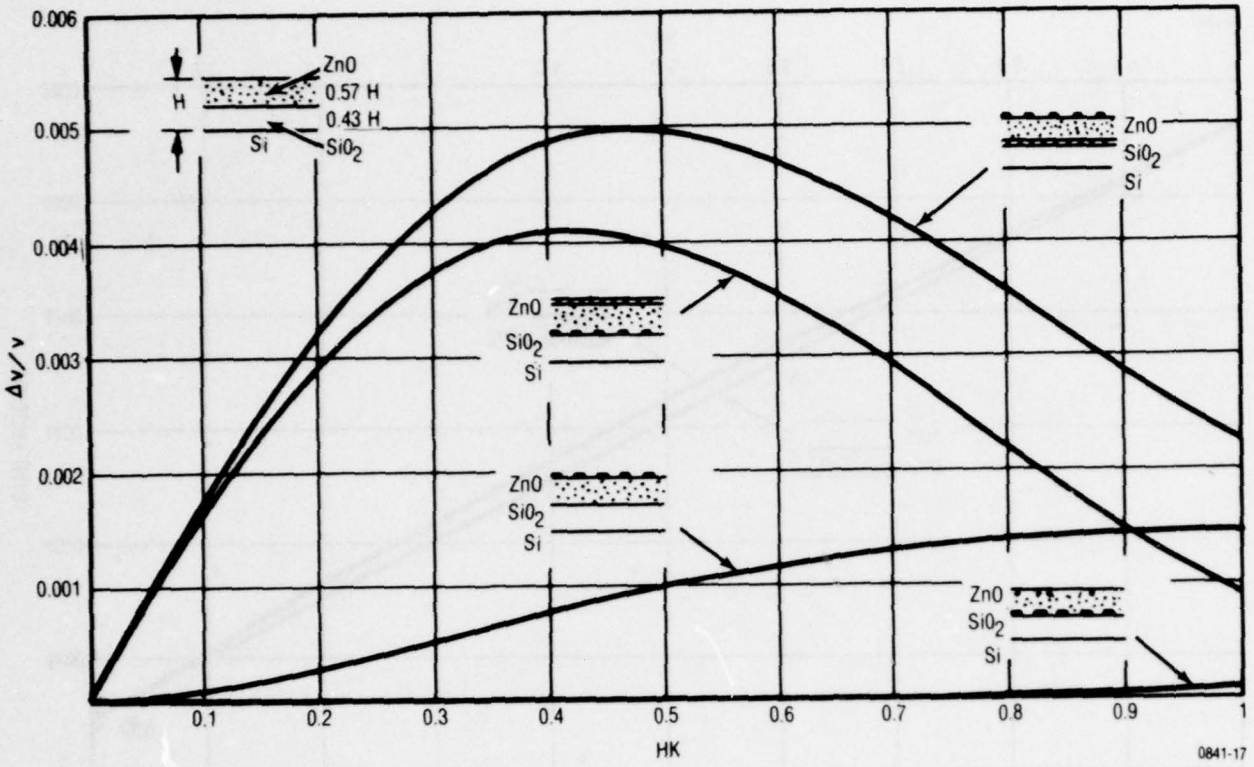


Figure 8. Calculated Conversion Efficiency ($\Delta v/v$) For C-ZnO/SiO_2/Si (001) [100] As a Function of Film Thickness-Wavenumber

The zinc oxide thickness corresponding to the most efficient transduction was in the 2.6 to 2.8 μm range. The theoretical coupling factor was predicted to be near 0.8%. The predicted conversion loss for a single transducer was less than 15 dB.

In order to minimize direct signal coupling from the input transducer to the output drain line through the substrate, a P+ diffused region in the silicon was placed directly beneath the interdigital transducer area. This diffused region was contacted directly to ground in order to eliminate any resistive paths for the electrical fields generated by the transducer.

4. MOSFET TAPS

The MOSFET tap structure design was similar to that of the previous program. Better tap topography for acoustic wave transmission was maintained by removing test points from within the tap area and maintaining a pattern symmetry with the oxide and metal regions. The overall tap aperture (MOSFET width) was 20 mils for a single tap. The overall width of the paired bi-phase taps was slightly over 40 mils.

A simplified cross-section through a MOSFET tap with the dimensions of the major structural features is given in Figure 9. The source, drain and gate-channel regions are shown together with the oxide and metal contact areas. A drawn channel length of 0.4 mil was designed which is normally reduced to approximately 0.2 mil because of lateral diffusion of the source and drain regions during wafer processing. The minimum gate to source and drain distance is 1 mil. The P-doped substrate is in the 14-22 ohm-cm range. The N+ diffusion depths are approximately 2.0 μm. The gate oxide is 1000 Å thick and a total oxide thickness of 2.15 μm is developed. The aluminum metallization is 1.45 μm in thickness.

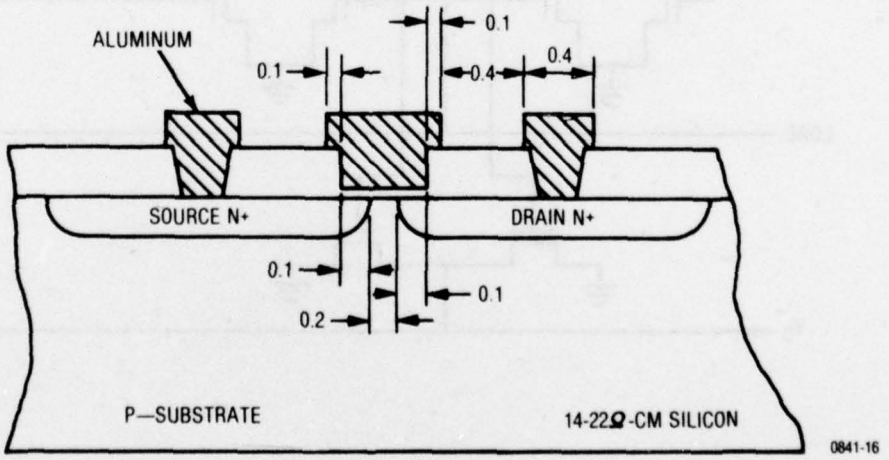


Figure 9. Geometry for Metal Gate N-MOSFET Acoustic Surface Wave Detectors

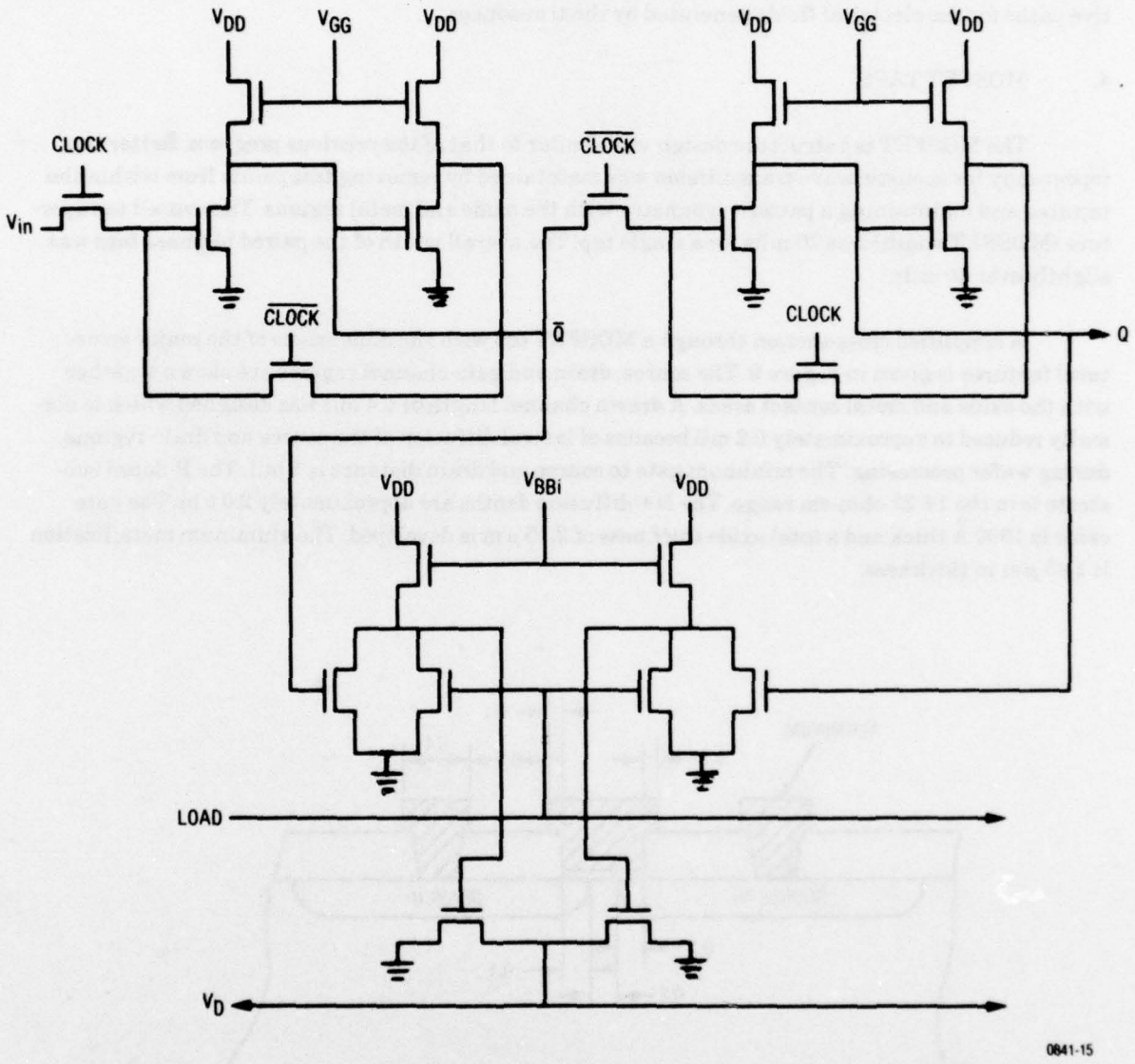


Figure 10. Shift Register and Load Inverter Cell Schematic

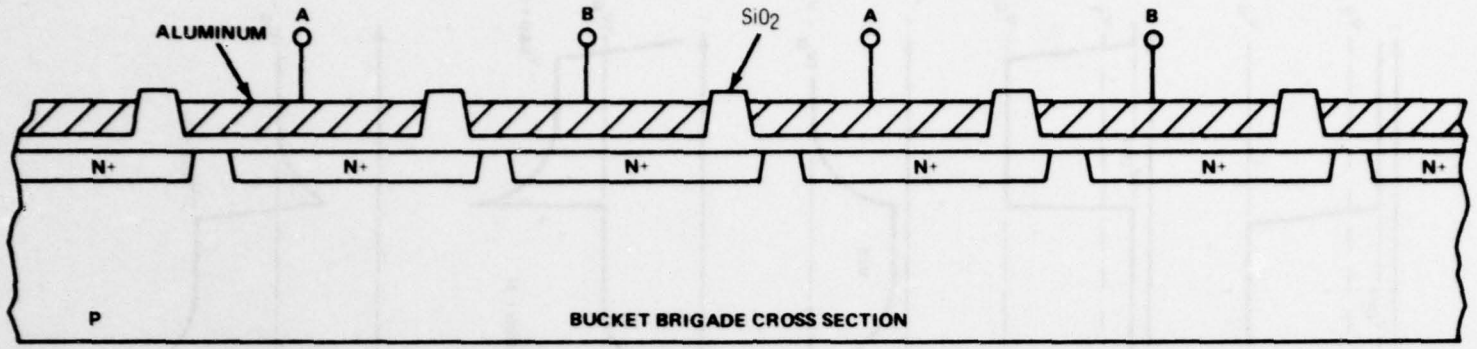


Figure 12. Bucket Brigade Cross Section

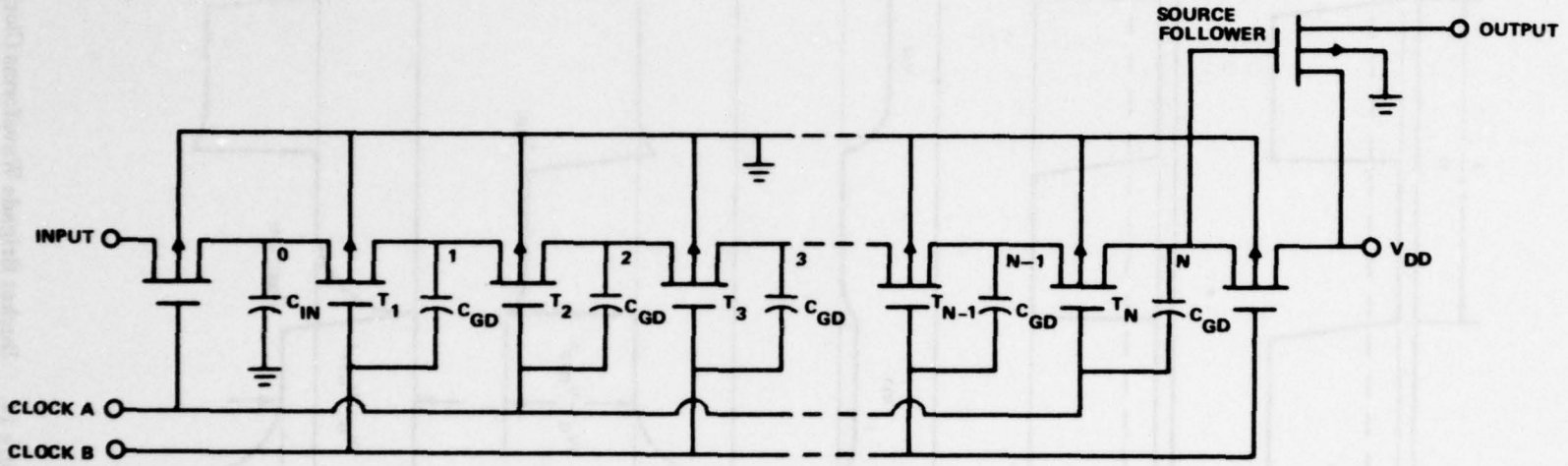


Figure 13. Bucket Brigade Schematic Diagram

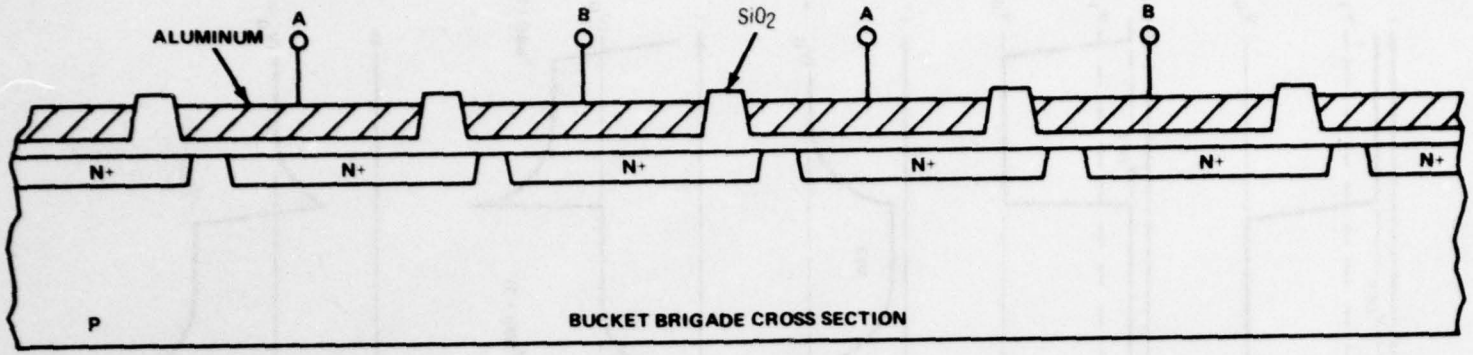


Figure 12. Bucket Brigade Cross Section

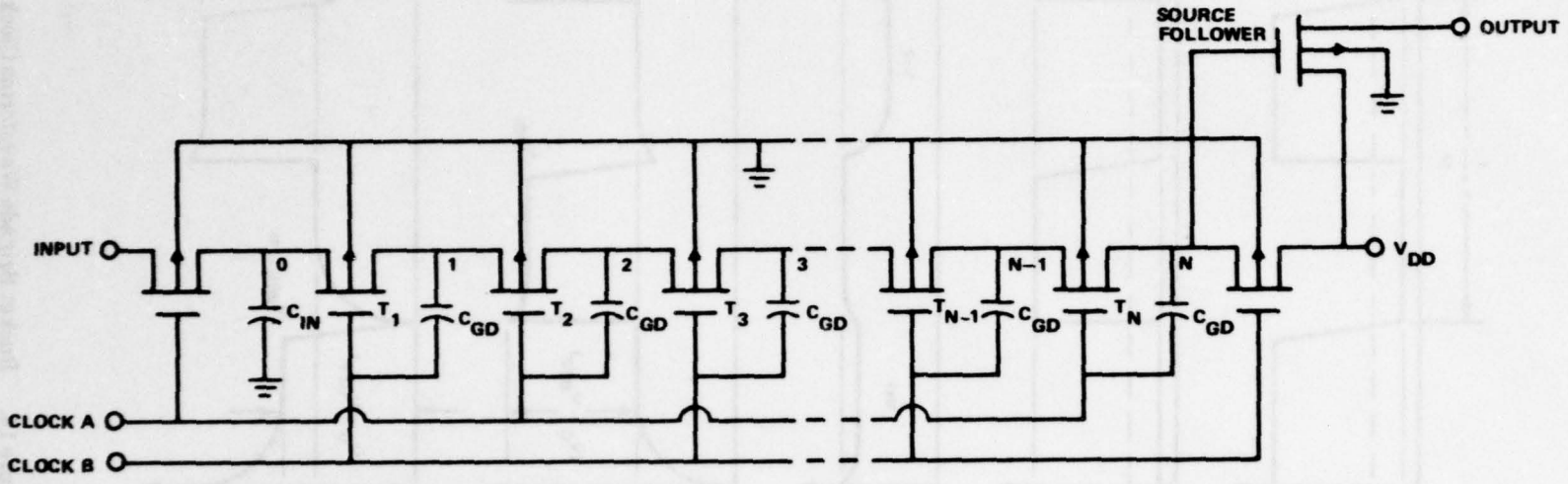


Figure 13. Bucket Brigade Schematic Diagram

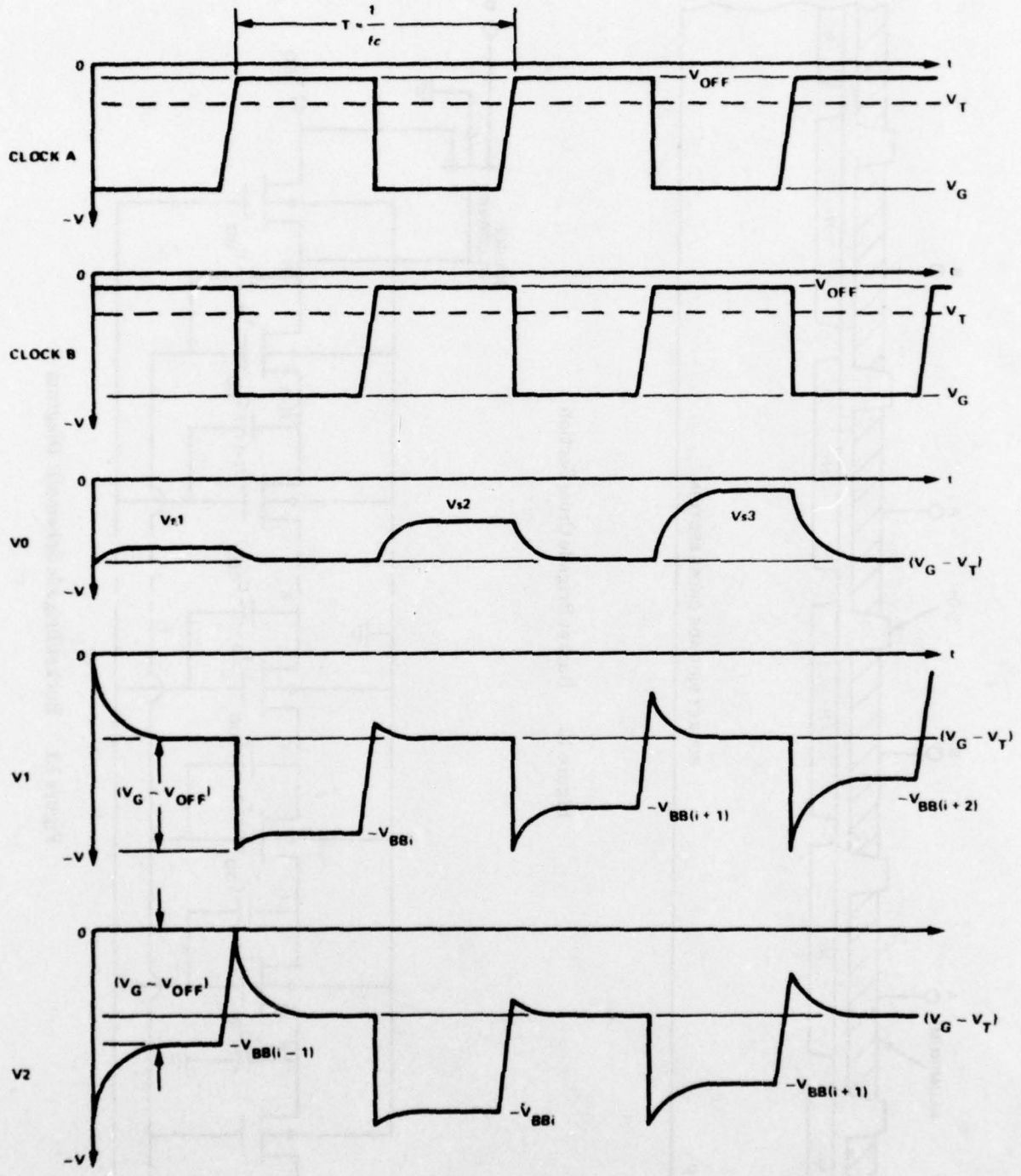


Figure 14. Bucket Brigade Waveforms Clock Pulses and First Three Stages for MOS Circuit

SECTION III

DEVICE LAYOUT AND MASK FABRICATION

The layout of the chip centers around the MOSFET detectors which are required to have a specific tap-to-tap spacing based upon the operational parameters and the acoustic velocity. These 31 taps are spaced on 18.8 mil centers spread across an area which is approximately 600 mils along the propagation direction and 50 mils in width. Each shift register element, containing several MOSFET devices, must address each tap pair. This restricts the dimension of a shift register element along the tap array to less than 18.8 mils unless fan-outs are used. The other dimension was not so restricted and was that necessary to accommodate the MOSFET device form factors. A 35 mil linear dimension normal to the tap array was required.

The bucket brigade device was considerably smaller in linear extent than taps and shift register and therefore it was necessary to use fan-out connections. The 62 MOSFET storage and transfer cells covered a linear extent of approximately 135 mils and a width of 10 mils. The load inverters were laid out below the bucket brigade devices.

The transducer electrode structures were placed at each end of the MOSFET tap array with sufficient distance to minimize direct electrical coupling to the tap output line. The contact pads were of minimum size to reduce parasitic capacitance.

The required bias, clock and ground lines addressing the active elements had their contact pads on the periphery of the chip. Test devices were placed in regions adjacent to the bucket brigade. There was also a ground line surrounding the chip.

The original layout of each device element was first done on gridded paper in pencil. Subsequently the device geometries were digitized and combined into basic cells necessary to make-up the total device. Each basic cell was layered representing the various processing steps and was displayed and examined on a CRT. Finally paper ink plots in various colors were made in an enlarged size for accurately checking device dimensions and line placements.

Figures 15, 16, and 17 show three of the basic cells used in developing the entire layout. Figure 15 shows the basic interdigital electrode with the split finger geometry and contact pad areas. Figure 16 is the basic cell which combines the MOSFET tap and digital static shift register structures. The entire bucket brigade and load inverter layout is shown in Figure 17. The cell also shows the fan-out lines for interconnection, test pads and input bias and clock lines.

It was necessary to compose the various mask layers from several cells like those shown in Figures 15 through 17. For example the cell shown in Figure 16 was used to generate the 31 detector taps and shift register using the Electromask stepper. In all, a total of 48 reticles at 10x size were used to generate the eight mask layers required to process the device. The mask identification numbers and their descriptions are given in Table 2.

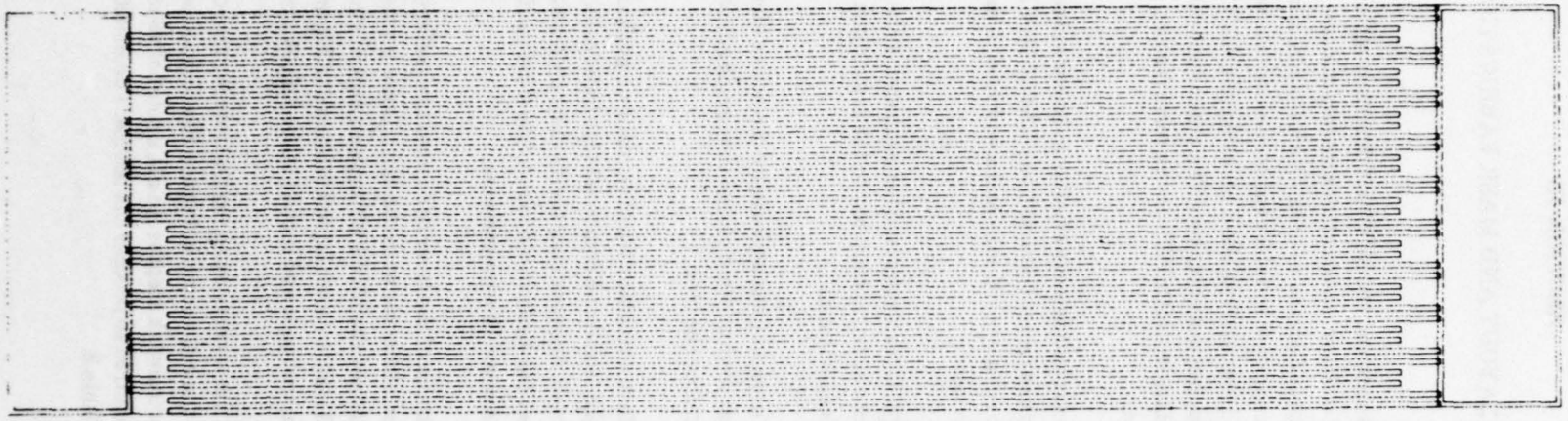


Figure 15. SAW Interdigital Electrode Transducer Structure

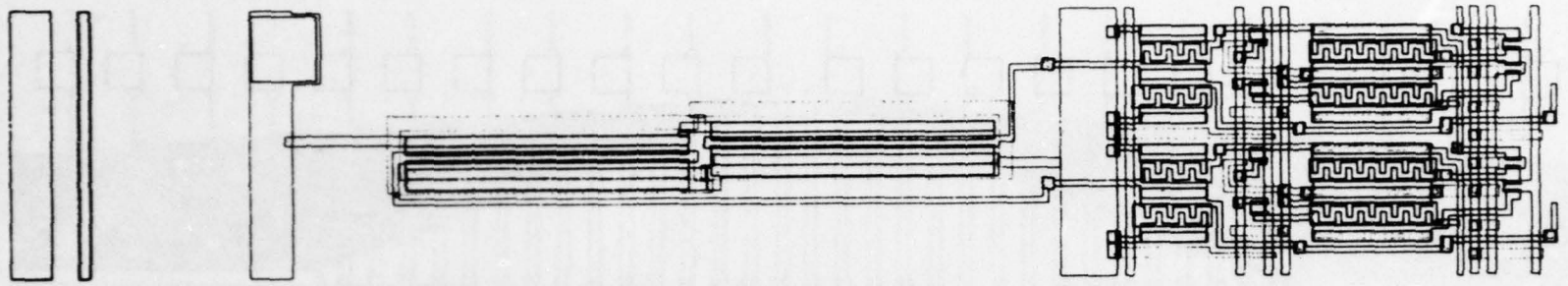


Figure 16. MOSFET Detector Tap and Shift Register Structure

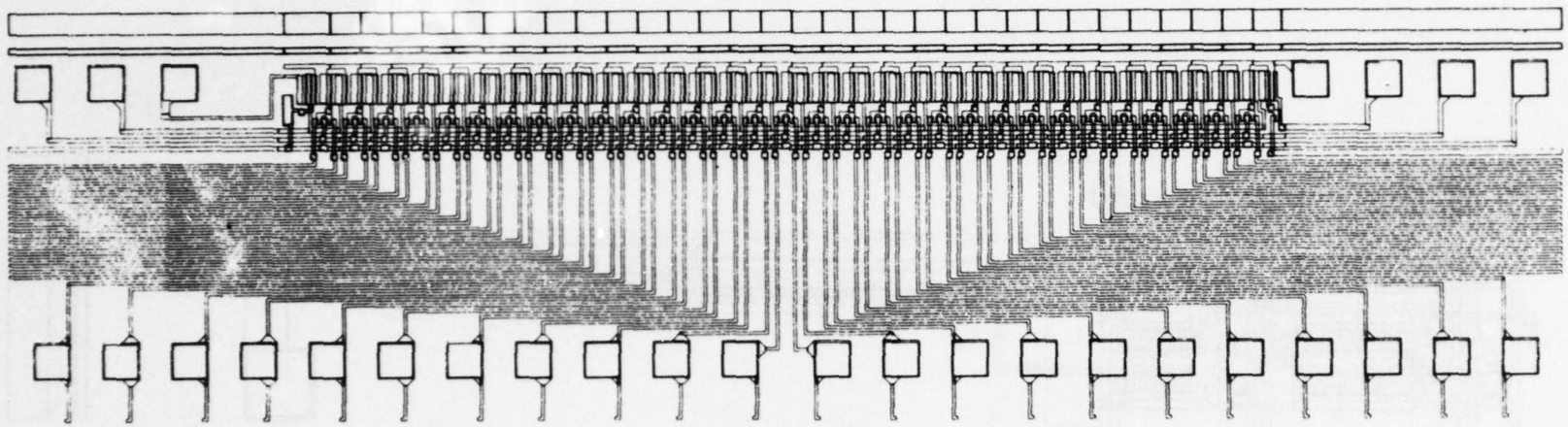
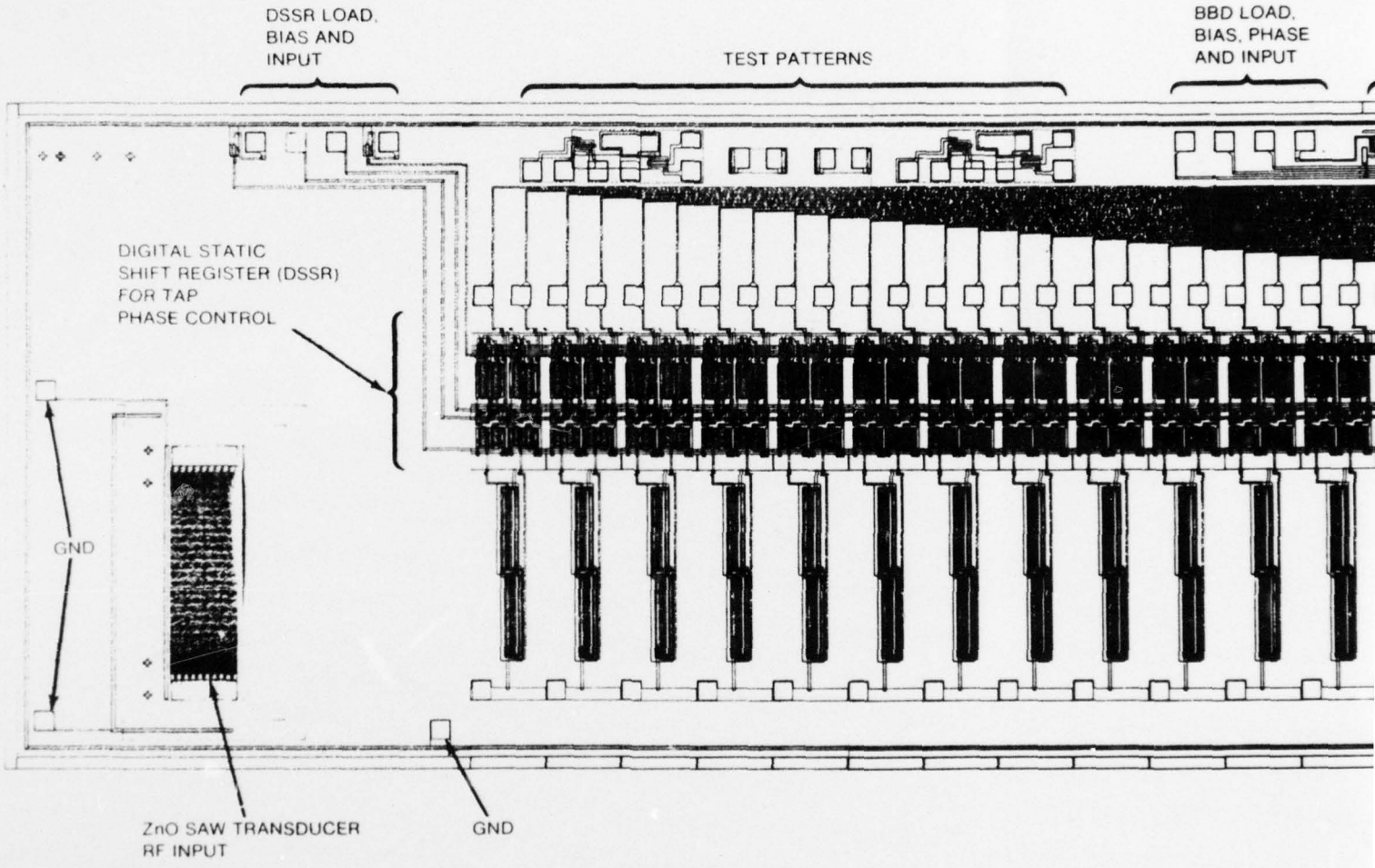


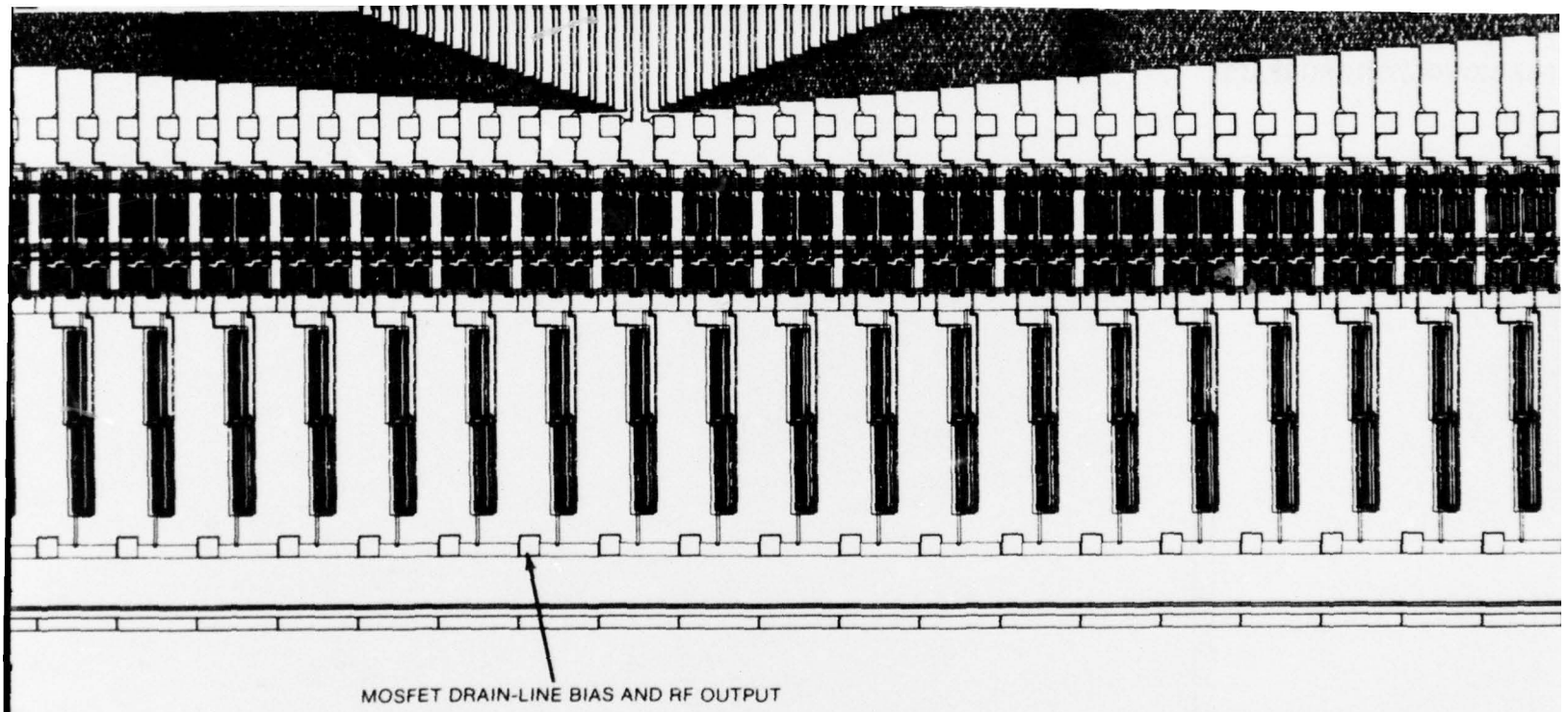
Figure 17. Bucket Brigade Device with Load Inverters and Fan-Out Leads

Figure 18 shows the entire layout of the chip and identifies pertinent features. The chip size is 810 mils by 160 mils. This size permitted the accommodation of three (3) columns of devices on a three inch wafer with a total of 37 devices possible on a single wafer.

TABLE 2. MASK LAYERS REQUIRED FOR PROCESSING THE MONOLITHIC SURFACE WAVE TRANSVERSAL FILTER

LAYER	DESCRIPTION
04	P+ Diffusion
05	N+ Diffusion
06D	Gate Definition
06A	Pre-ohmic
08	Metal Definition
11	Transducer Electrode
12	Transducer Metal
09	Passivation Cut


DSSR LOAD, BIAS AND INPUT
TEST PATTERNS
BBD LOAD, BIAS, PHASE AND INPUT
DIGITAL STATIC SHIFT REGISTER (DSSR) FOR TAP PHASE CONTROL
GND
ZnO SAW TRANSDUCER RF INPUT
GND


MOSFET DRAIN-LINE BIAS AND RF OUTPUT

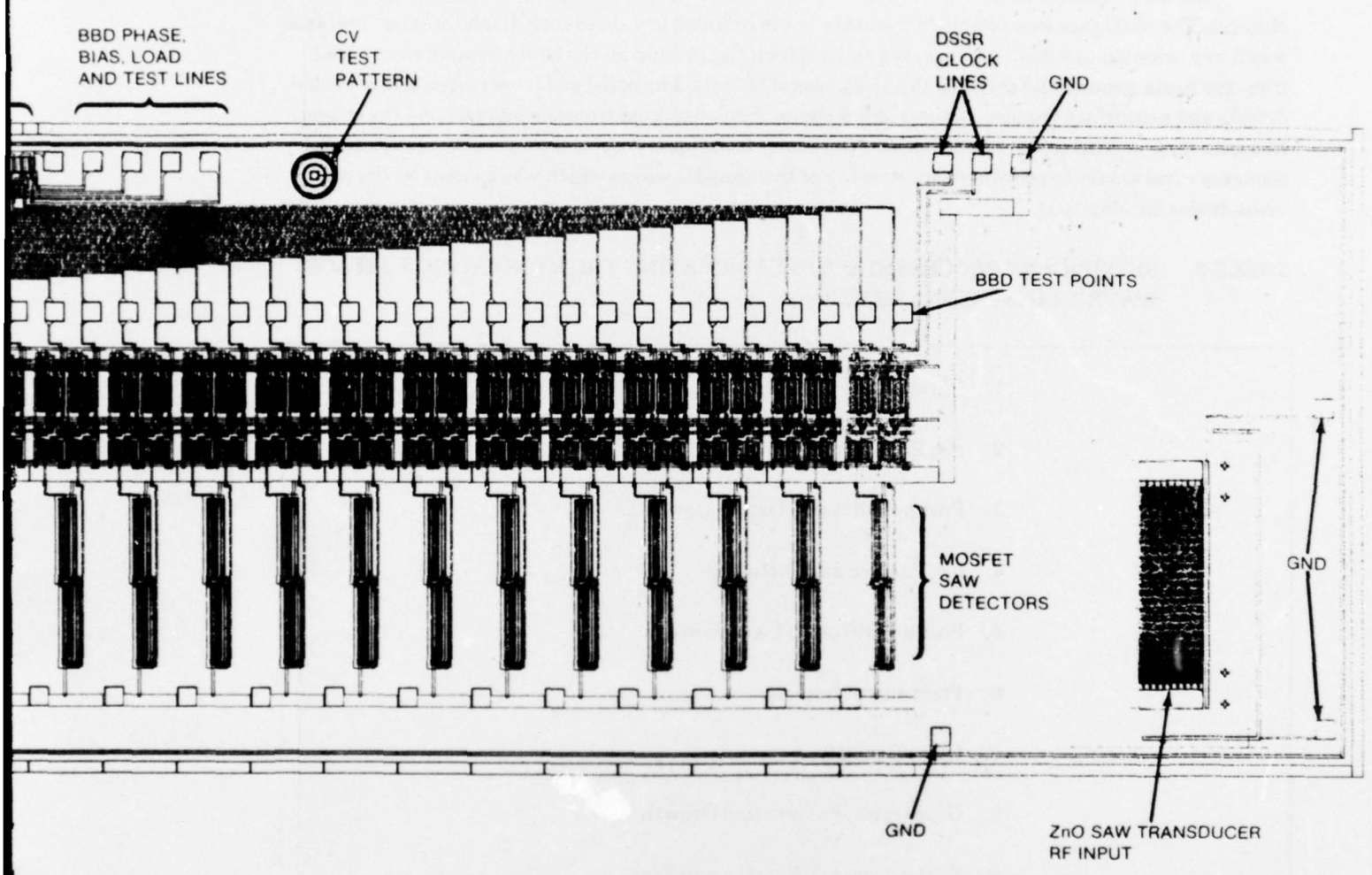


Figure 18. ZnO Si-MOSFET Surface Wave Transversal Filter

SECTION IV

WAFER PROCESSING

An (001) oriented silicon boule, doped with boron was grown for the resistivity range 14-22 ohm-cm. The (001) face was established and the boule rounded to a three inch diameter. The (100) face was X-ray oriented to within 0.25 degrees and a ¾ inch flat ground on the boule. Wafers were sliced from the boule, ground and polished to a thickness of 20 mils. The polished face was free of any visible defects and subsurface damage. Two wafers were randomly selected from the lot of 40 and the orientation accuracy verified using a Laué backscatter X-ray technique. A special concern for orientational accuracy is necessary to prevent beam steering of the acoustic waves which was evident on the previous device development.

TABLE 3. SIGNIFICANT PROCESS STEPS IN FABRICATING THE MONOLITHIC SURFACE WAVE TRANSVERSAL FILTER

1. Initial Oxide Growth
2. P+, Pattern and Diffusion
3. Post p+ Diffusion Oxide Growth
4. n+, Pattern and Diffusion
5. Post n+ Diffusion Oxide Growth
6. Field adjust implant
7. Glass Deposition
8. Gate Oxide, Pattern and Growth
9. Silicon Contact, Pattern and Etch
10. Aluminum Deposition, Pattern and Sinter
11. Passivation Glass Deposition
12. Gold Back
13. Transducer Fabrication
14. Aluminum Pad Contact, Pattern and Etch.

An existing metal gate CMOS process was modified to produce the N-channel circuitry required for the transversal filter. The significant process steps required are shown in Table 3. There were no special processes developed. The characteristic structural parameters of the NMOS devices are given in Table 4.

TABLE 4. CHARACTERISTIC STRUCTURAL PARAMETERS OF THE NMOS CIRCUITRY

Starting Material:	(001), Boron Doped, 14-22 ohm-cm
Final Chip Thickness:	20.0 Mil
Field Oxide Thickness:	12,500 Å
Gate Oxide Thickness:	1000 Å
Implant Density	1×10^{16}
n+ Diffusion ρ_s:	15-25 Ω/sq
Junction Depth:	~0.1 mil
p+ Diffusion ρ_s:	15-25 Ω/sq
Junction Depth:	~0.1 mil
Aluminum Thickness:	14,500 Å
Passivation Oxide	9000 Å

The zinc oxide transducer processing was done on the wafers after the MOSFET processing was completed and the wafer was glass passivated. The wafer was aluminized (1000Å) and the interdigital electrodes replicated using standard photolithographic techniques. The zinc oxide was dc triode sputtered through an aperture mask over the electrode structures. The sputtering conditions are given in Table 5. Additional information regarding ZnO film deposition and properties is found in reference 17. The final steps in the processing of the zinc oxide transducers were 1) the deposition of 1000 Å of aluminum on the wafer 2) photoreplication of the aluminum metal plane directly over the interdigital electrode region, and 3) a final etch definition of the zinc oxide around the electrode region.

TABLE 5. SPUTTERING CONDITIONS FOR ZINC OXIDE FILM LAYER TRANSDUCERS

Pressure	3.0 μm
Gas Mixture	90% Ar - 10% O_2
Substrate Temperature	200° C

TABLE 5. SPUTTERING CONDITIONS FOR ZINC OXIDE FILM LAYER TRANSDUCERS (CONTD)

Deposition Rate	1.0 μm/hr.
Target-Substrate Distance	4 cm
Target	4.0 inch diameter ZnO pressed cake
Target Voltage	2.0 KV
Target Current	50 mA

The wafer processing was completed with the etching of the glass passivation and zinc oxide to expose the electrical contact pads.

A photograph of the total wafer and a closeup view are shown in Figures 19 and 20, respectively. This is how the wafer appears with all the semiconductor processing completed. The wafers are normally processed in lots of ten with 37 complete devices on each wafer.

The first wafer lot processed did not have good devices on it. This was traced to a design/processing error in the implant step. On the second lot of ten wafers, two lots of three each were processed to establish a proper implant dosage level. On the second lot this level was established and the final four wafers were processed. From two of these wafers came the devices which were rf tested.

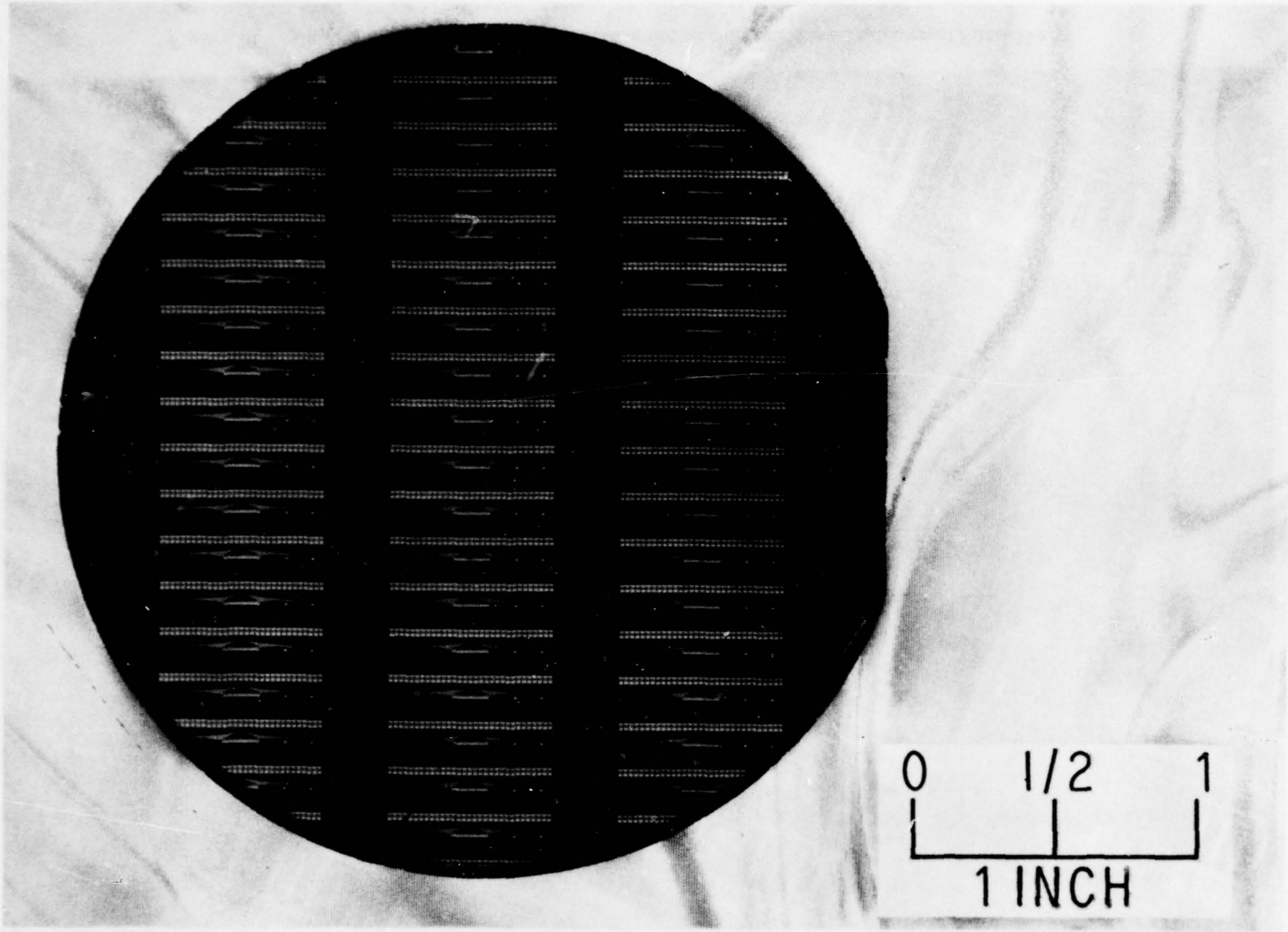


Figure 19. Monolithic Surface Wave Transversal Filter Wafer

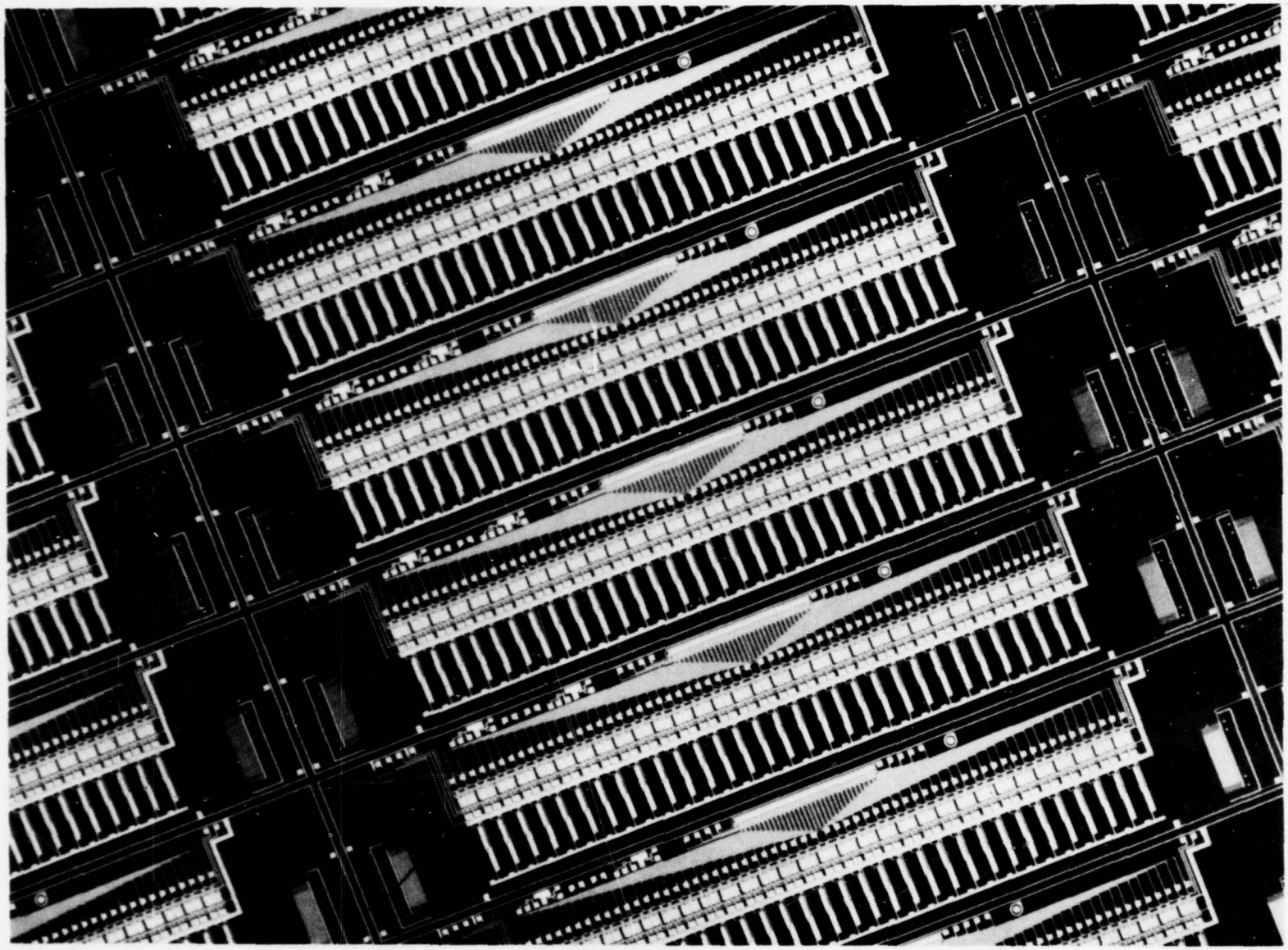


Figure 20. Closeup Photograph of Portion of Monolothic Surface Wave Transversal Filter Wafer

SECTION V

WAFER CHARACTERIZATION

1. DC ELECTRICAL TESTING

Prior to sawing a processed wafer, it is important to electrically test and visually examine all devices on the wafer to determine which are most suitable for packaging. The bulk of the electrical testing was done by making use of MICARL's Fairchild Sentry 600 Tester. This machine is capable of performing appropriate electrical measurements on the MOSFET circuitry of all dice on the wafer and printing out the results. A specially made probe card was used to contact all necessary input and output pads of the semiconductor circuits. The ability of the bucket brigade and shift register to clock and maintain appropriate voltage levels was tested. The leakage current level from the 31 parallel connected MOSFET tap drains was measured. A computer printout of data rated the semiconductor circuits of each device. Number data was transferred to a gridded map and the good devices identified. These devices were subsequently visually inspected under a 200x microscope to identify any obvious mechanical damage.

Additional data was obtained through off-line tests using both the logic circuit devices and the test transistors. Average device data obtained on good wafers is summarized in Table 6.

The change of threshold voltage with substrate bias, "body effect", was examined. This occurs in n-channel devices and proved to be a problem in device operation. Figure 21 shows the threshold field as a function of substrate on devices from two of the wafers. The threshold voltage increased from near the 1.0 volt level to above 3.0 volts for a substrate bias from zero to −5 volts. This cuts down the effective voltage seen by the various semiconductor circuitry.

TABLE 6. SUMMARY OF DEVICE ELECTRICAL PARAMETERS

Threshold Voltage	1.0 - 1.25 Volts
Field Inversion Voltage	>15V
Field Oxide Capacitance	$\sim .02$ pf/mil^2
Mobility	~ 700 cm^2/V-sec
Drain Leakage Current	$>2 \times 10^{-8}$ A

Channel conductance, g, was also measured by placing the MOSFET devices in saturation and measuring the drain current as a function of drain voltage. The conductance is a function of gate voltage. A plot of drain current versus voltage is shown in Figure 22. As the drain current increases with gate voltage the conductance also increases. Measurements on 0.4 mil channel length devices showed a conductance change from 5 micromhos at drain currents of 0.5 mA to 3.5 micromhos at a

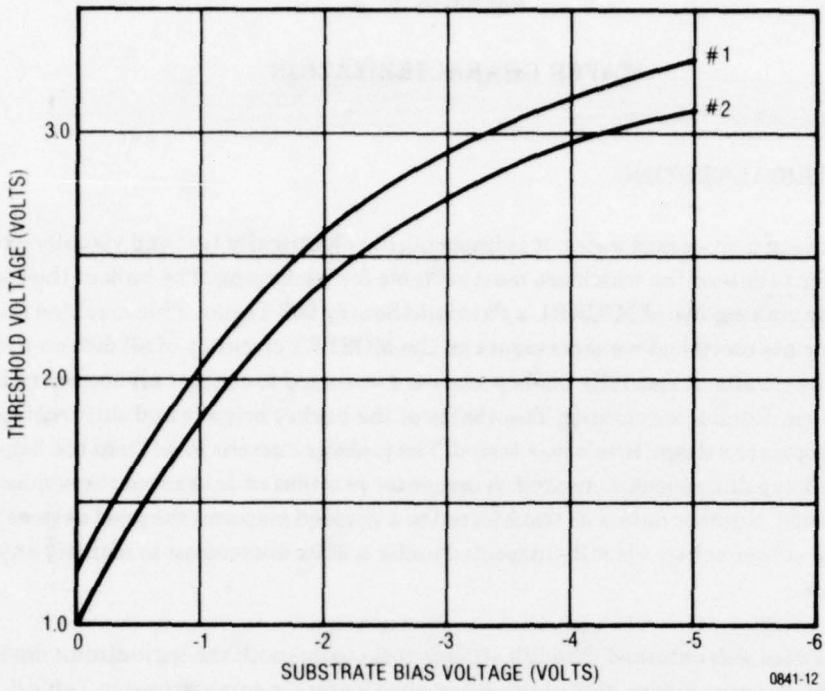


Figure 21. Change of Threshold Voltage With Substrate Bias in NMOS Device

drain current of 3.5 mA. This represents a linear relationship between the drain current and conductance with a ratio value of 100 volts.

Figure 23 shows scope traces for tests performed on the operation of the bucket brigade and shift register. In this test, a single bit time level of approximately five volts was presented to the bucket brigade at time 1 with 0 volts presented at subsequent times. The BB trace shows the appearance of the 5 volt input level 31 bit times later. The scope probe monitored the bucket brigade test point output and thus shows an attenuated version of the bucket brigade waveform as modified by the input levels. Simultaneous with the bucket brigade clocking, a digital one level was applied to the shift register at time 1 with digital zero levels at subsequent times. The SR trace shows the effect of that one level at bit time 31. The SR monitor point was the last test pad above the last SR stage located within the chip. This SR test point is physically connected to one gate of the thirty first MOSFET tap pair. The scope trace shows the effect of the digital one level pulling the MOSFET tap gate to zero.

The two upper pictures of figure 23 are for tester loops with single bit time "one" levels applied to the BB and SR. The BB test point output is clocked on BB phase one in the top picture and phase two in the middle picture. The two test loops were devised to attempt to determine the correct clock phase to stop shifting the bucket brigade for best amplitude output.

The third picture shows the effects of a 0100000000000101111111111111101 pattern into the shift register. The slow rise to zero level after a one level was caused by loading of the test point by the measuring system.

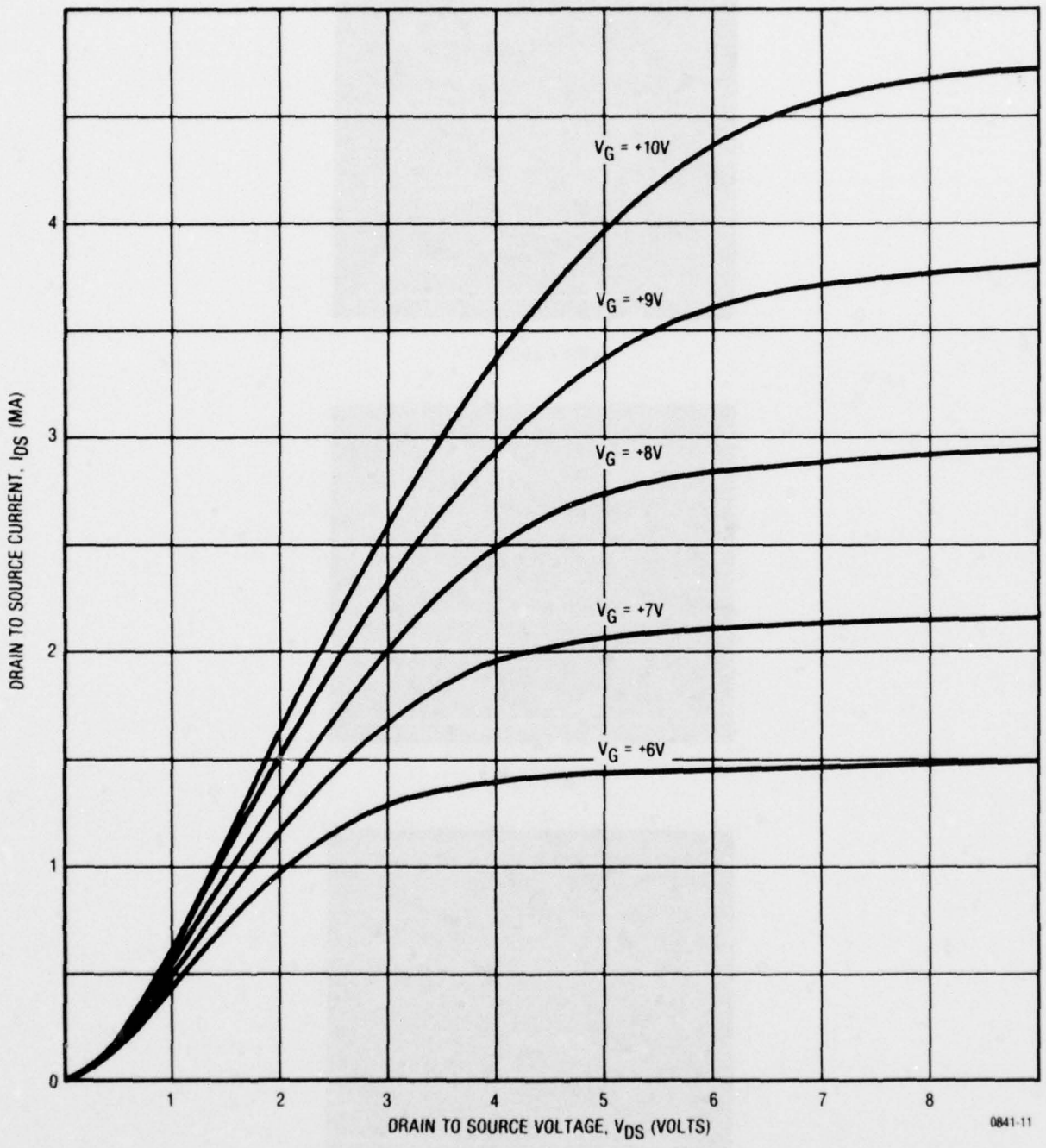
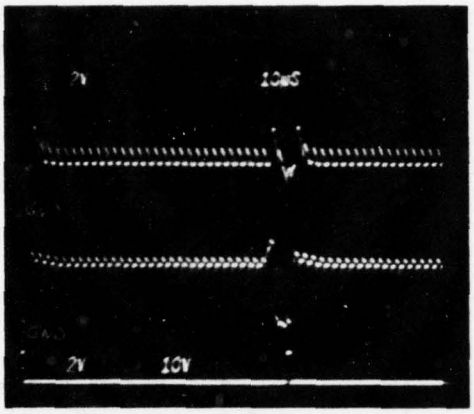
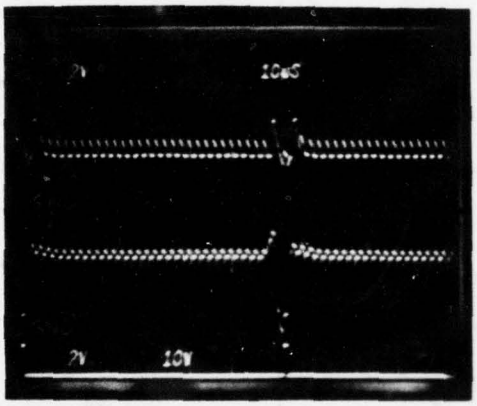


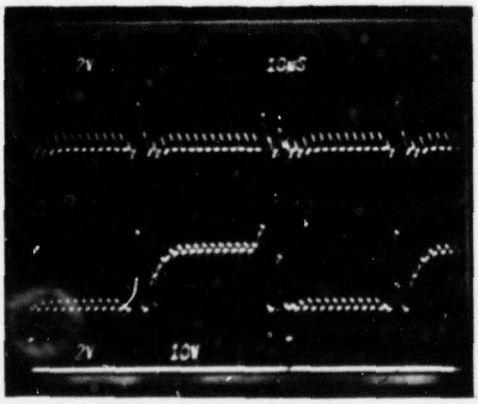
Figure 22. **Drain Current as a Function of Drain-to-Source Voltage and Gate Voltage for NMOS Device**



'B6KV' LOOP 1



'B6KV' LOOP 2



'B6KV' LOOP 3

0841-10

Figure 23. Scope Traces of Bucket Brigade and Shift Register Operation

"Off line" tests were also performed on the wafers after the Sentry test to better establish the integrity of the BB, SR and MOSFET taps. These tests were performed on each device and consisted of 1) sampling a sine wave input into the BB and noting the reproduced, chopped, delayed sine wave out of the BB test point 2) shifting a pattern into the SR and monitoring at the SR test point previously mentioned and 3) a test on the MOSFET taps to verify the I_D measurement made by the Sentry tester. From the "off line" tests a wafer map of the expected good devices was made and used to select dice for assembly and test.

On the devices selected, the bucket brigade operated well for signal input levels under 4.0 volts at a 1 MHz rate. For signal levels above this level, the output showed limiting at the 4.5 volt level. This was a manifestation of the "body effect" described earlier and limited the dynamic range of the bucket brigade. The shift register circuitry showed good operation up to 10 MHz rates for the devices selected.

Transducers were visually inspected and a sampling of dc electrical measurements made. The visual criteria were: 1) no shorts or opens in the interdigital finger pattern and 2) zinc oxide films with high transparency and an optically smooth surface preferred. The dc criterion was for a high resistivity film in excess of 10^6 ohm-cm. The devices passing the semiconductor tests were ranked according to their optical film quality. The best devices were then chosen for packaging.

2. WAFER YIELD

As indicated in the previous section there were processing problems with the early runs and it was necessary to adjust the ion implant dosage to achieve the desired MOSFET characteristics. Two of the final four wafers were those used to package devices for rf testing and to evaluate yield factors. Based on the dc electrical and visual testing the yield of good devices on the first wafer was 54% and the yield on the second device was 45%. This is an exceptionally good yield for such a large MOSFET die. In the previous development, which had a smaller area of active devices, the yields were in the 20% range. The high yield for such a complex device in its first development is considered a tribute to the type of technology and the caliber of people at Motorola which were dedicated to the development.

SECTION VI

DEVICE FABRICATION

1. WAFER SCRIBE

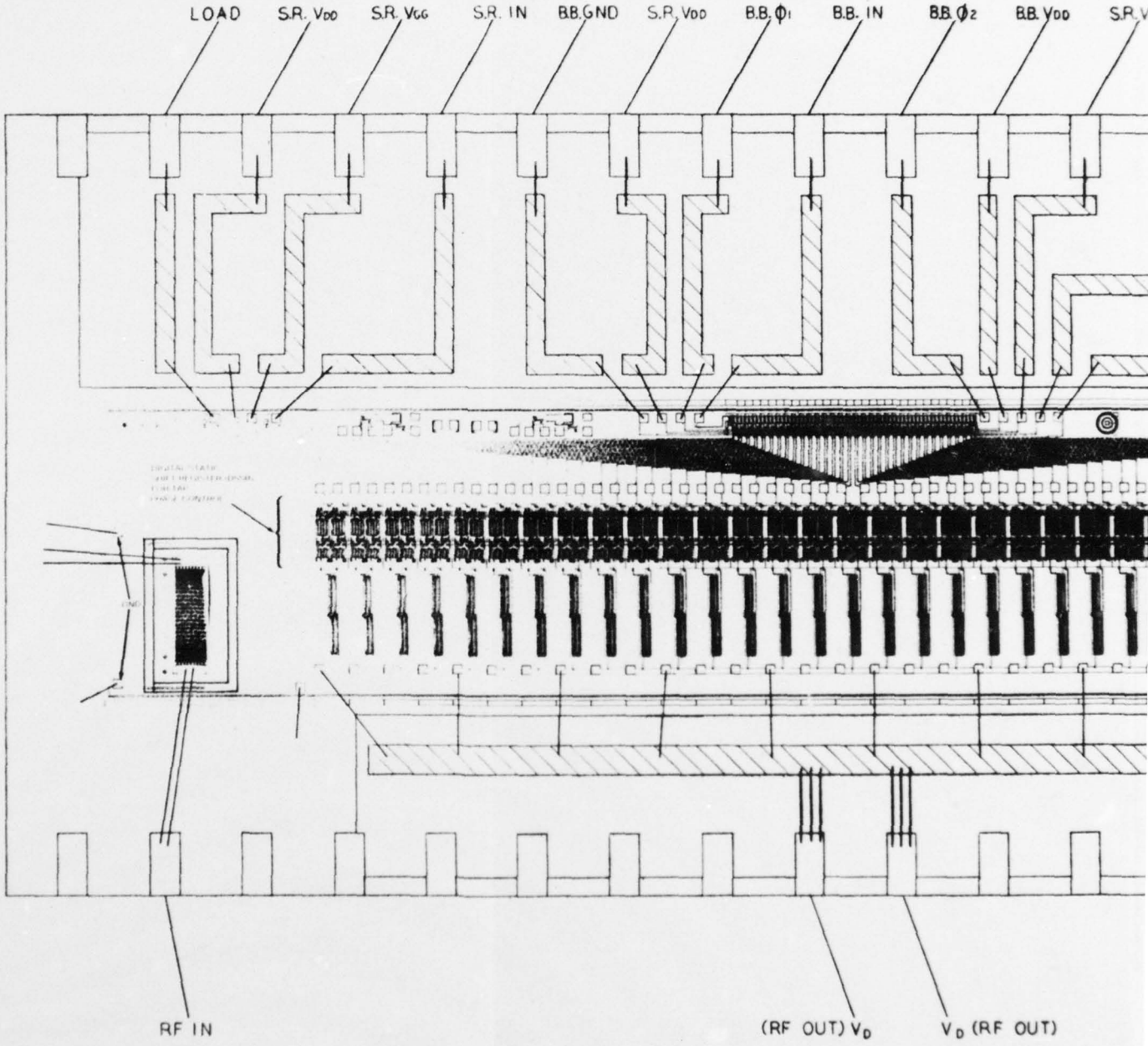
After the potentially good die were identified on the wafer, a Tempress dicing saw was used to cut the wafer. The thin diamond impregnated blade of the saw rotates at 18,000 rpm while a continuous flow of D.I. water rinses the surface. The cutting speed reduces edge chipping to an absolute minimum, while the D.I. water rinse eliminates silicon dust contamination on the surface. Die identity was maintained by packaging the devices in small groups.

2. DEVICE PACKAGING

A commercially available all metal flat-pack, the Isotronics IP 1065, was used to house the transversal filter chip. A pin out configuration was chosen to accommodate all necessary dc and rf interconnections to the package pins. To allow proper routing of the dc and rf voltages and maintain short wire bonds, two aluminum oxide substrate circuit boards were used. The alumina substrates had thick film gold metallization for the conductor paths. The positioning of the alumina substrates and the device chip in the package are shown in Figure 24. The upper alumina substrate routes all of the bias, clock and ground connections to the bucket brigade and shift register. The other alumina substrate is used to route the drain voltage and rf output of the MOSFET taps. The transducers are connected directly to the package pin leads and the ground connections of the transducer structure go directly to the bottom of the metal package.

3. DEVICE ASSEMBLY

The alumina substrates and the MOSFET chip were secured to the bottom of the flat pack using a high conductivity silver adhesive made by Acme Chemical (E-KOTE 3030). The adhesive provides a strong bond but allows substrate removal by dissolving the adhesive in trichloroethane (TCA). After the ceramic substrate and MOSFET chip had been attached to the package and the adhesive cured, the device was ultrasonically wire bonded using 0.001 inch aluminum wire. Using an ultrasonic wire bonder avoids the damaging temperatures presented by ordinary thermo-compression (TC) bonding techniques. The MOSFET final step before the lid was attached was to place an acoustic absorber on the surface of the chip at each end behind the ZnO tansducers. The absorber eliminates surface waves that reflect from the ends of the chip, thereby reducing the level of spurious outputs. The material used as the absorber is made by Dow Corning (RTV 3144). Finally, the lid was attached to the package after all dc and rf testing was completed. The package could be hermetically sealed as required. Figures 25 and 26 show the packaged device die. A total of 25 die were packaged and tested.


LOAD
S.R. V_{DD}
S.R. V_{GG}
S.R. IN
B.B. GND
S.R. V_{DD}
B.B. ϕ_1
B.B. IN
B.B. ϕ_2
B.B. V_{DD}
S.R. V
RF IN
(RF OUT) V_D
V_D (RF OUT)

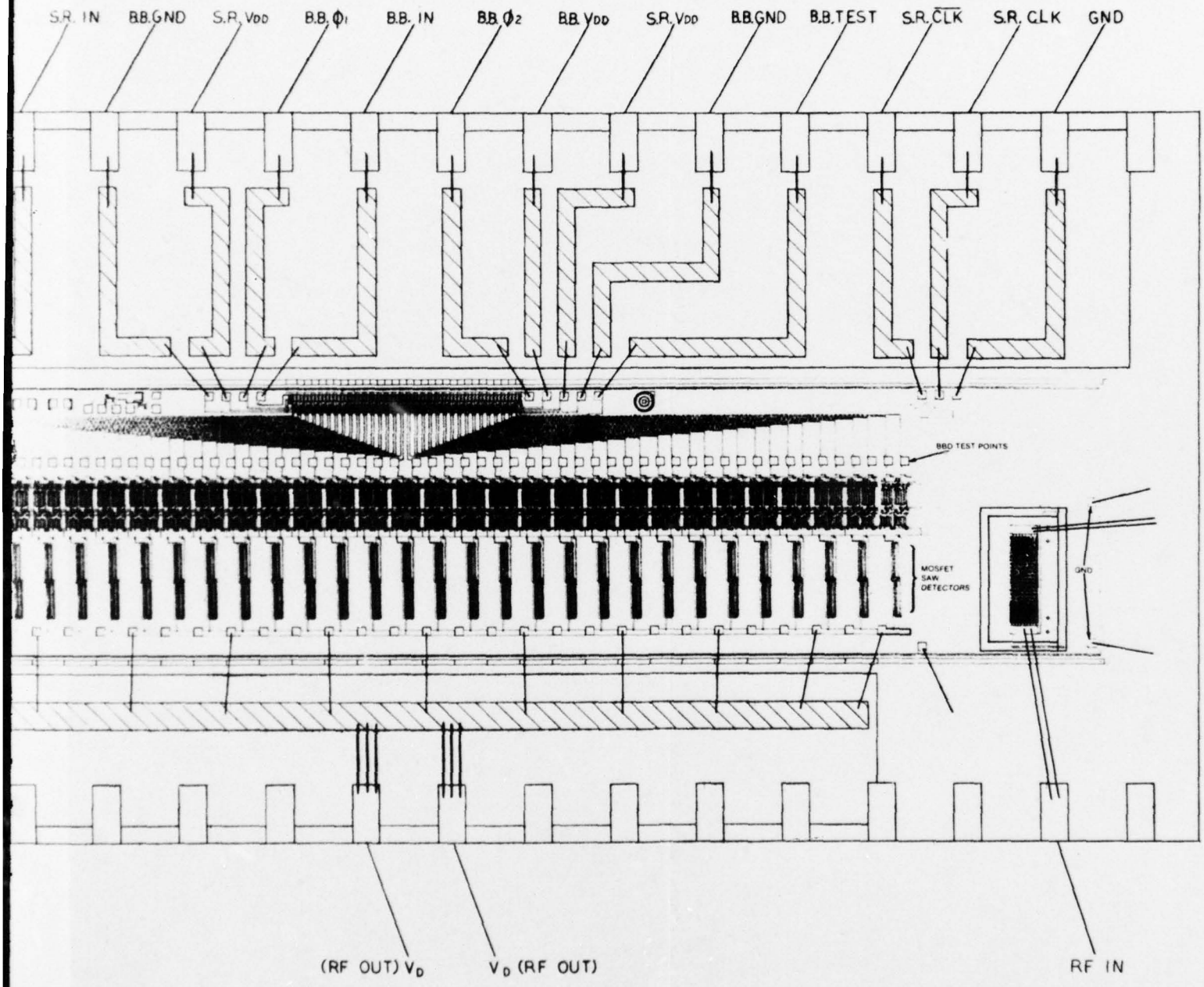


Figure 24. Package Configuration for Transversal Filter

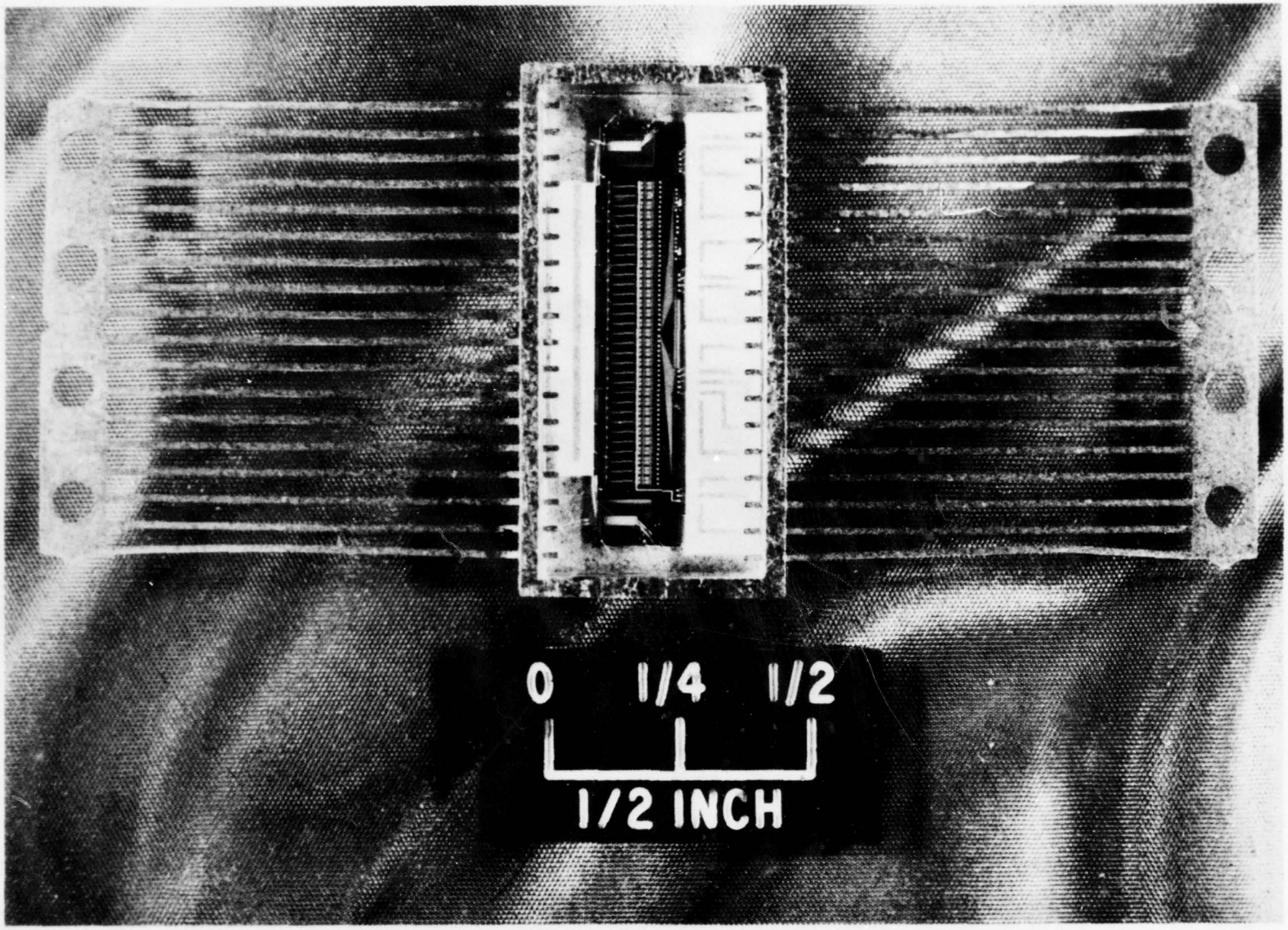


Figure 25. Packaged Monolithic Surface Wave Transversal Filter

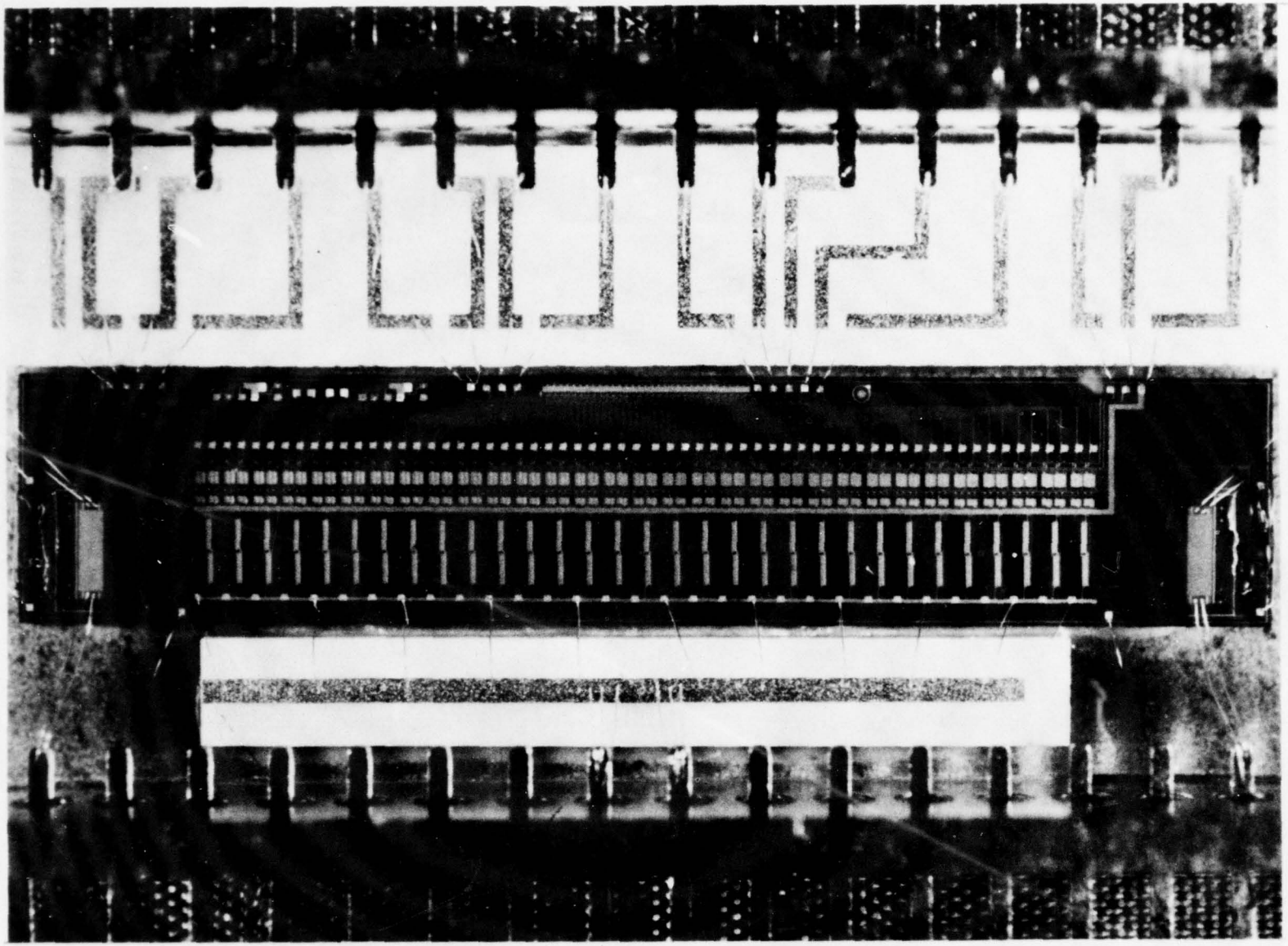


Figure 26. Close-Up View of Packaged Monolithic Surface Wave Transversal Filter

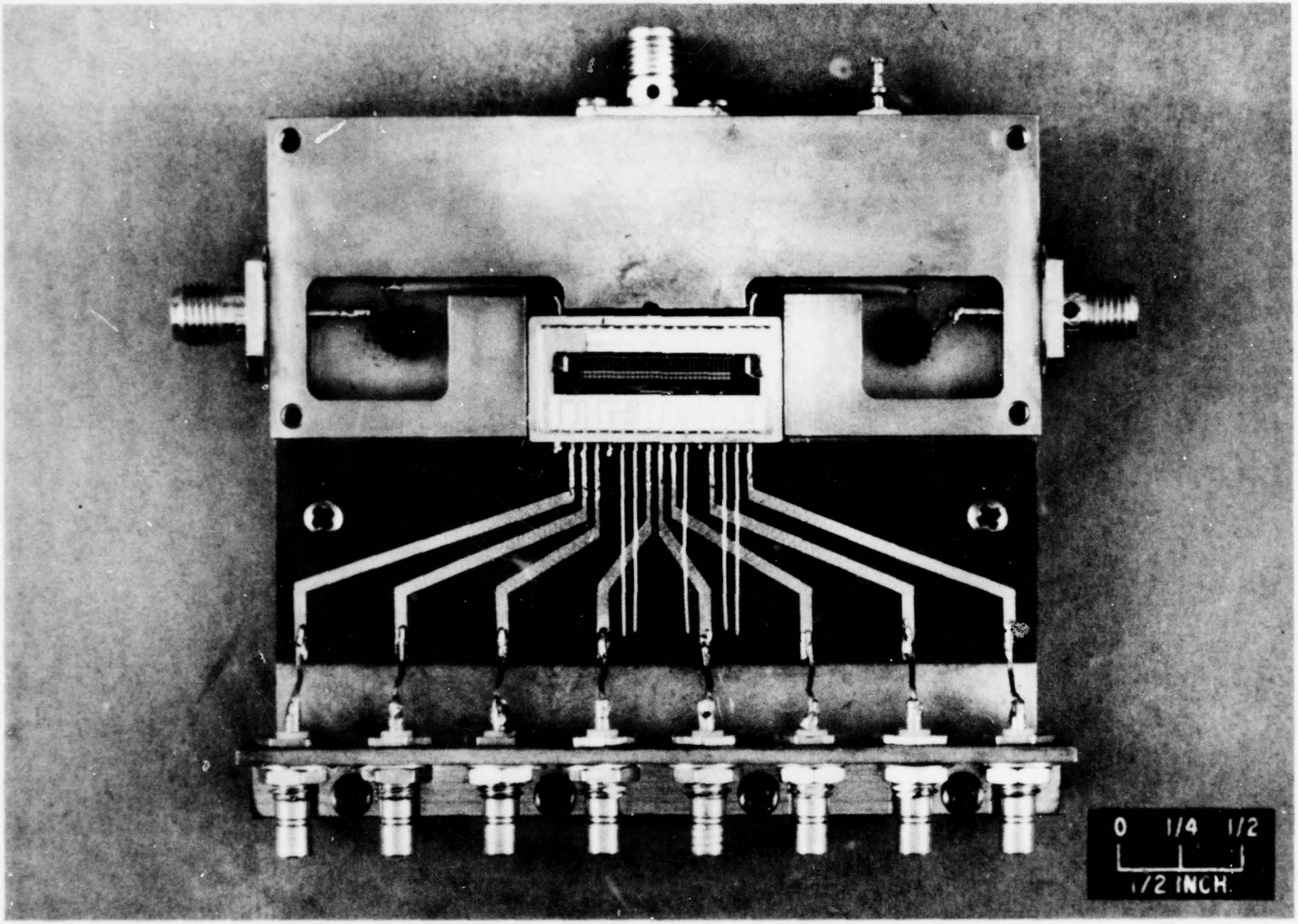


Figure 27. Top View of Package Holding Fixture for RF Tests

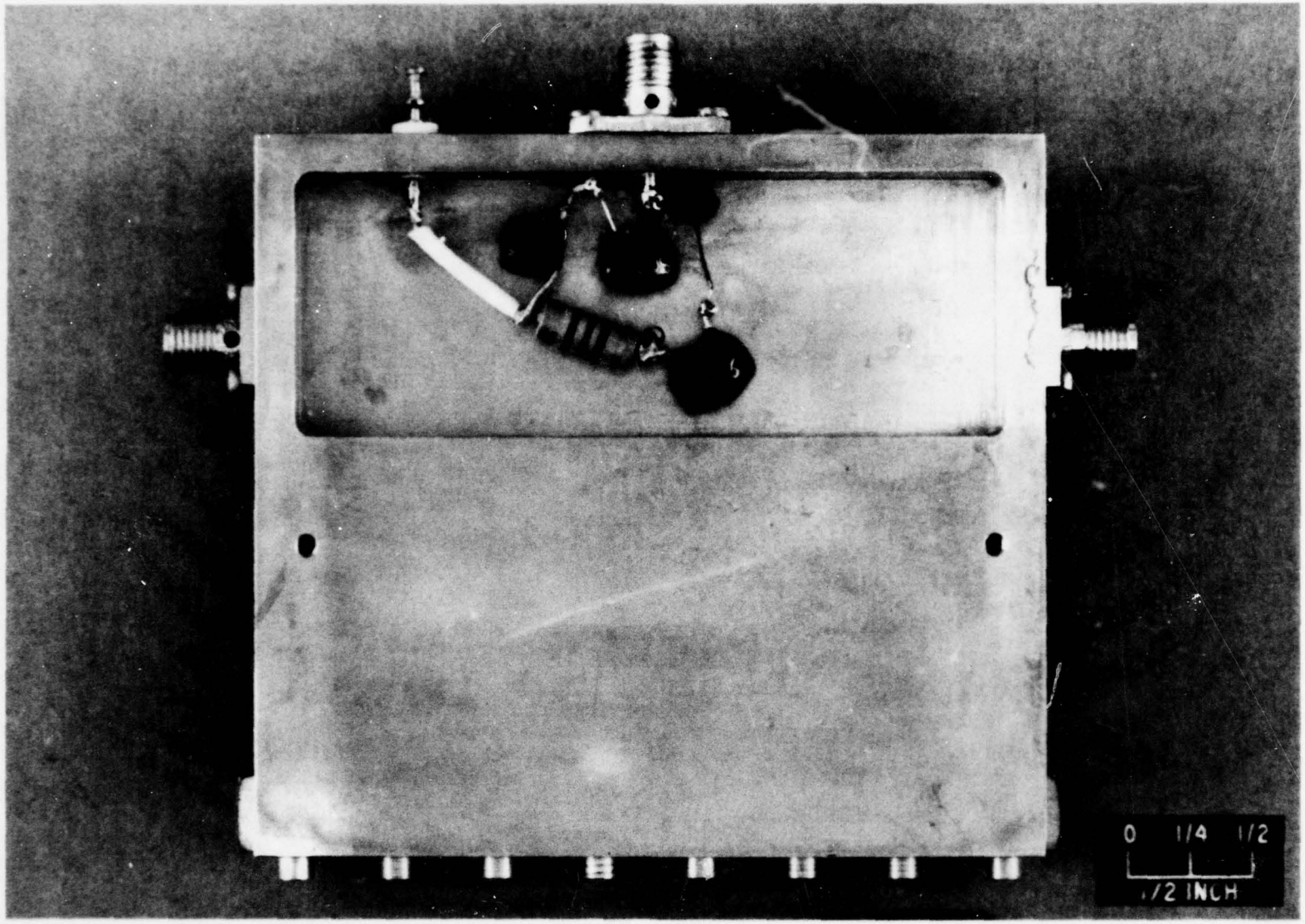


Figure 28. Bottom View of Package Holding Fixture for RF Tests

4. PACKAGE HOLDER

The device package holder serves the purpose of 1) providing a simple means of connection to dc and rf sources, 2) accommodating rf matching networks while maintaining input-output isolation, and 3) heat sinking. The brass test fixture with top and bottom views shown in Figures 27 and 28, respectively, provided these functions. A microstrip circuit board with soldered package pin connections and miniature cable connectors handled the clocking inputs. Part of the bias voltages were connected directly to package leads. The input channels to the zinc oxide transducers are evident along with isolated compartments for the matching which was a series coil. The detector output lead was fed directly through a small hole to the opposite side of the package holder where a matching circuit could be accommodated. The matching element cavities were shielded by a metal plate. Rf connectors were standard OSM. It was possible to achieve a 90 dB level of isolation between input and output with the device operating in this package holder.

SECTION VII

PROGRAMMABLE TEST SET

In order to evaluate the phase and amplitude programmability features of the monolithic surface wave transversal filter it was necessary to develop controlled logic and rf signal inputs to the device. It was decided to develop a digitally controlled test set because it best met the criteria for ease of signal control and versatility of signal output. The test set was designed using standard piece-parts and breadboard housing. An overall schematic representation of the test mode is shown in Figure 29; its operation is described below.

The test set was designed to produce an rf signal of 100 MHz which could be biphase modulated by individual bit switches and was controlled in amplitude by the adjustment of resistors in the individual bit times. The analog level is set in the surface wave device by inserting an analog serial stream along with appropriate clocks.

Consistent with bucket brigade performance, the insertion rate of the analog voltage is one microsecond per sample. Therefore, it takes 31 microseconds to set the voltages in the bucket brigade. A complete cycle of the operation requires approximately 50 microseconds, allowing 5 for the rf and 45 for the analog control.

Two signal generators are required, one operating at 100 MHz and the other producing 5 microsecond pulses at a repetition rate of 20,000 pulses per second. All timing and signals are generated from these two generators, and they do not need to be synchronized. A timing diagram is shown in Figure 30.

The 100 MHz supplies the clock for the square wave generator, F/F−1, and is divided to give the necessary frequencies of 10 MHz, and 1 MHz. An exclusive/OR gate in combination with F/F−1 generates the 100 MHz biphase modulated signal as determined by the ORed output of the 31-bit shift register. A "zero" out of the shift register produces one phase, while a "one" produces the opposite phase as illustrated in Figure 30.

The signal is fed through a buffer amplifier into an MC 1590 which is a monolithic amplifier with dc gain control capabilities. The dc control is generated simultaneously with the phase control bits.

The 31-bit shift register is the heart of the phase and amplitude control. Through the use of the 31-input diode NOR gate, a "one" input is generated only when all outputs are zero. However, at the time this input is generated, F/F-2 is reset and it controls gates that stop all clocks going into the 31-bit shift register. Therefore, the shift register is stopped with all "0"s in the output. The shifting of the "1" input is reinitiated upon any change of the 20 kHz pulse generator. Positive going sets F/F-2 and opens gate 3 so that 10 MHz is supplied to the clock input of the shift register, causing a "1" to be shifted at a 10 MHz through until all "0"s cause F/F-2 to be reset in 3.1 microseconds.

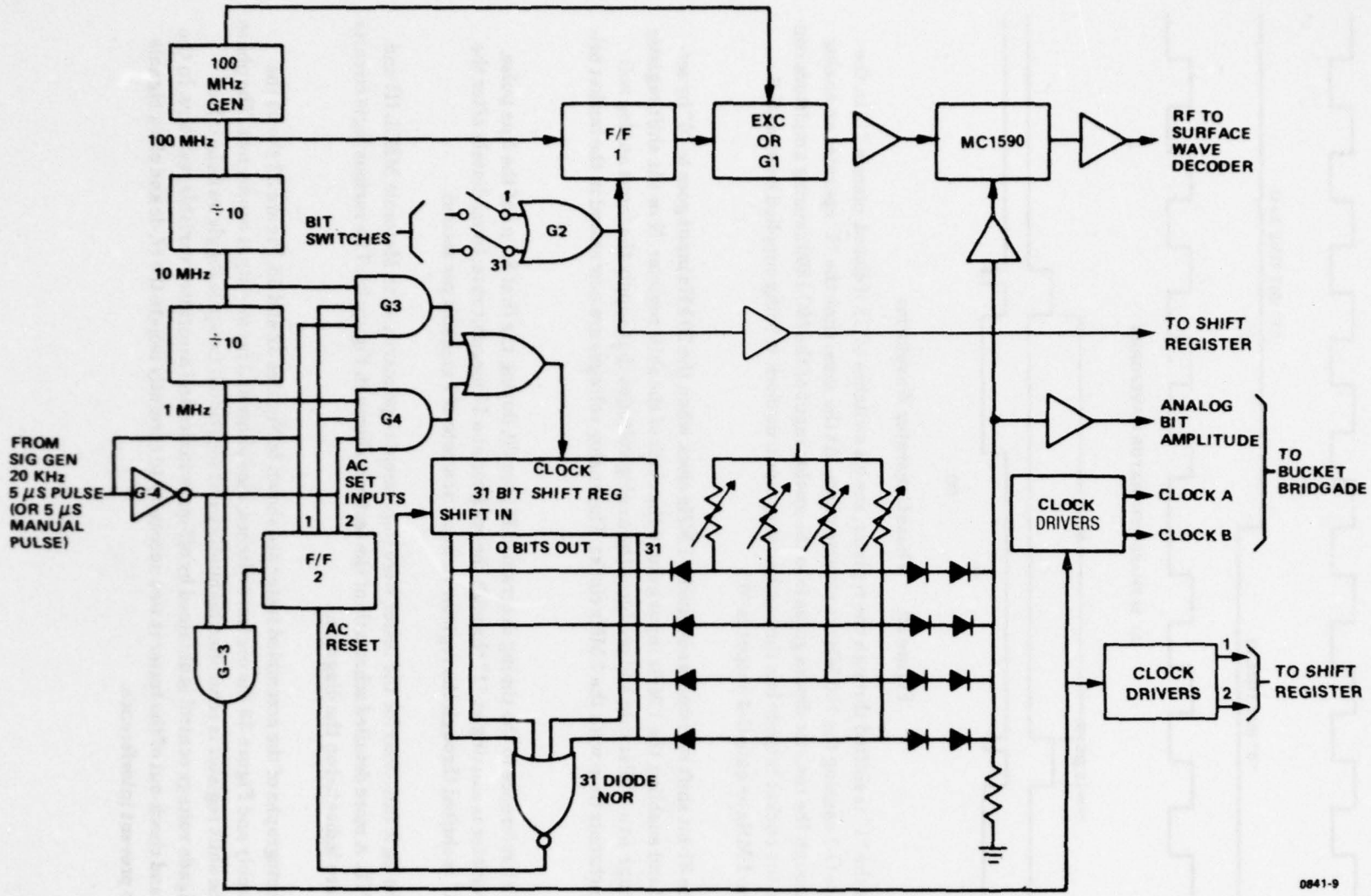


Figure 29. Analog and Digital Tester

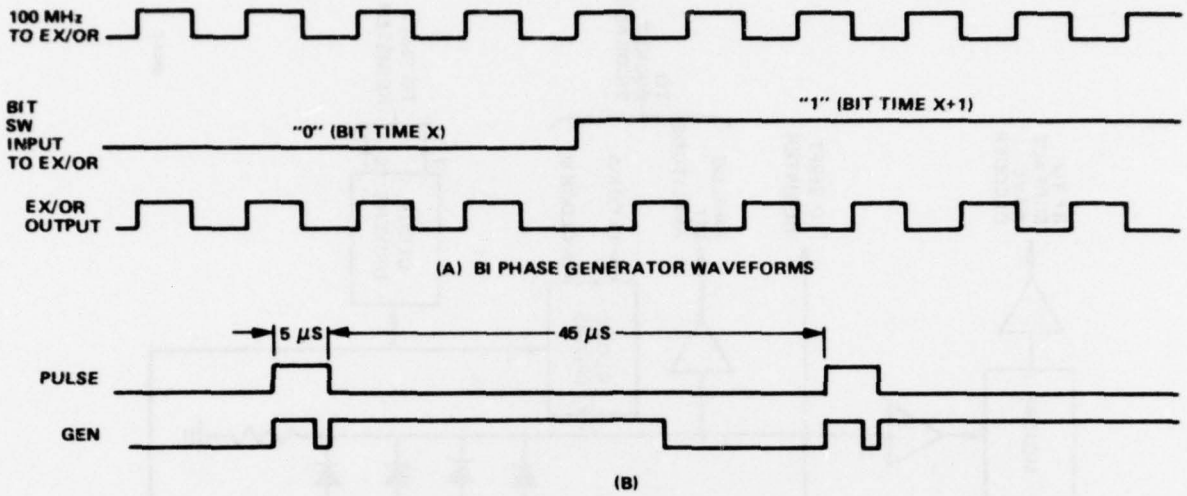


Figure 30. Phase Generator Waveforms

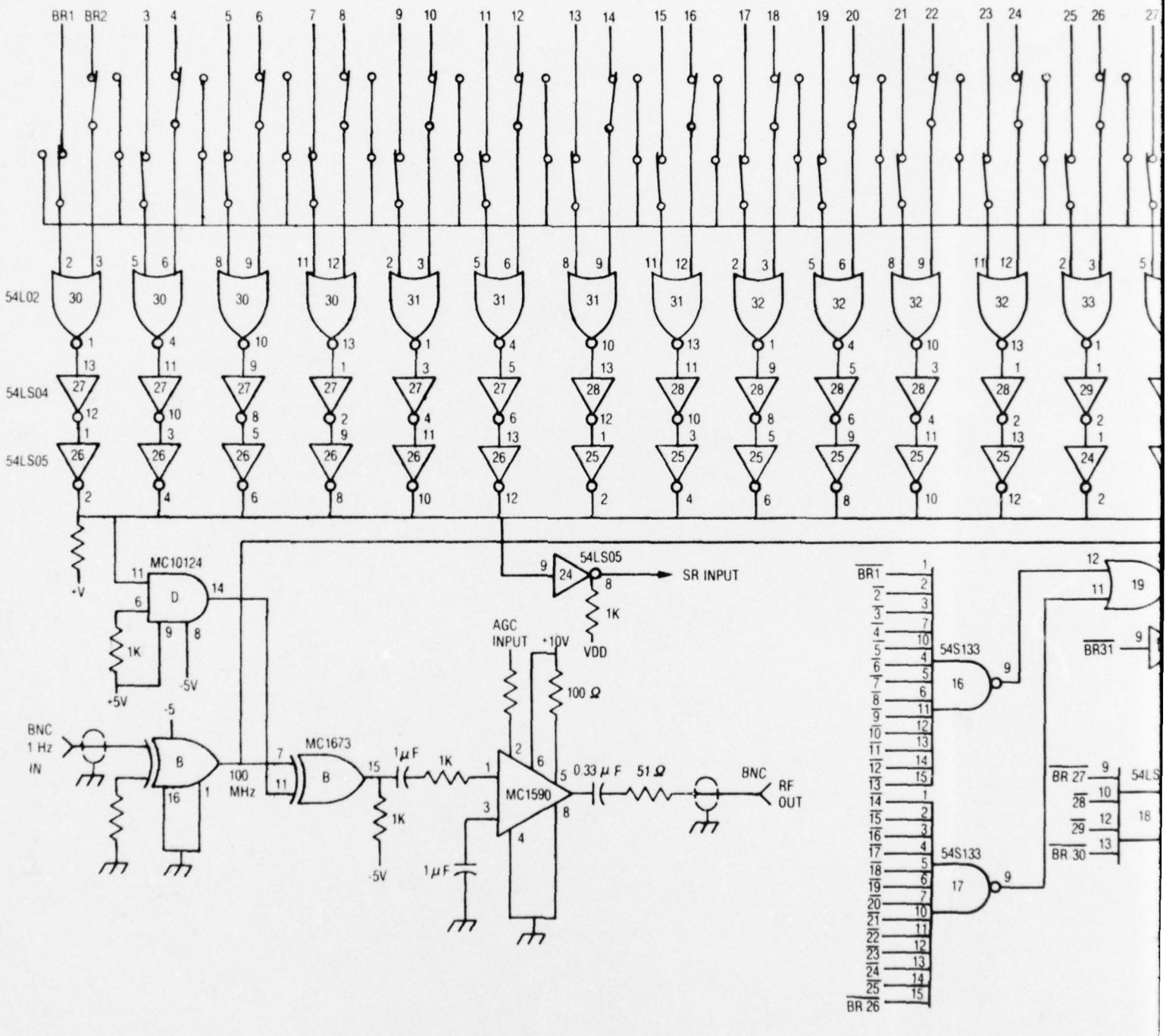
As the "1" is shifted through the register, the bit switches of G2 if closed, place a "1" in the EX/OR gate G-1 causing the 100 MHz to reverse phase. At the same time the "1" operates an analog voltage through the resistor diodes gates into the analog input of the MC 1590 causing amplitude control. While the bucket brigade has the same analog input, no clock is being supplied because G-3 inhibits the 1 MHz as gate G-4 output is "0".

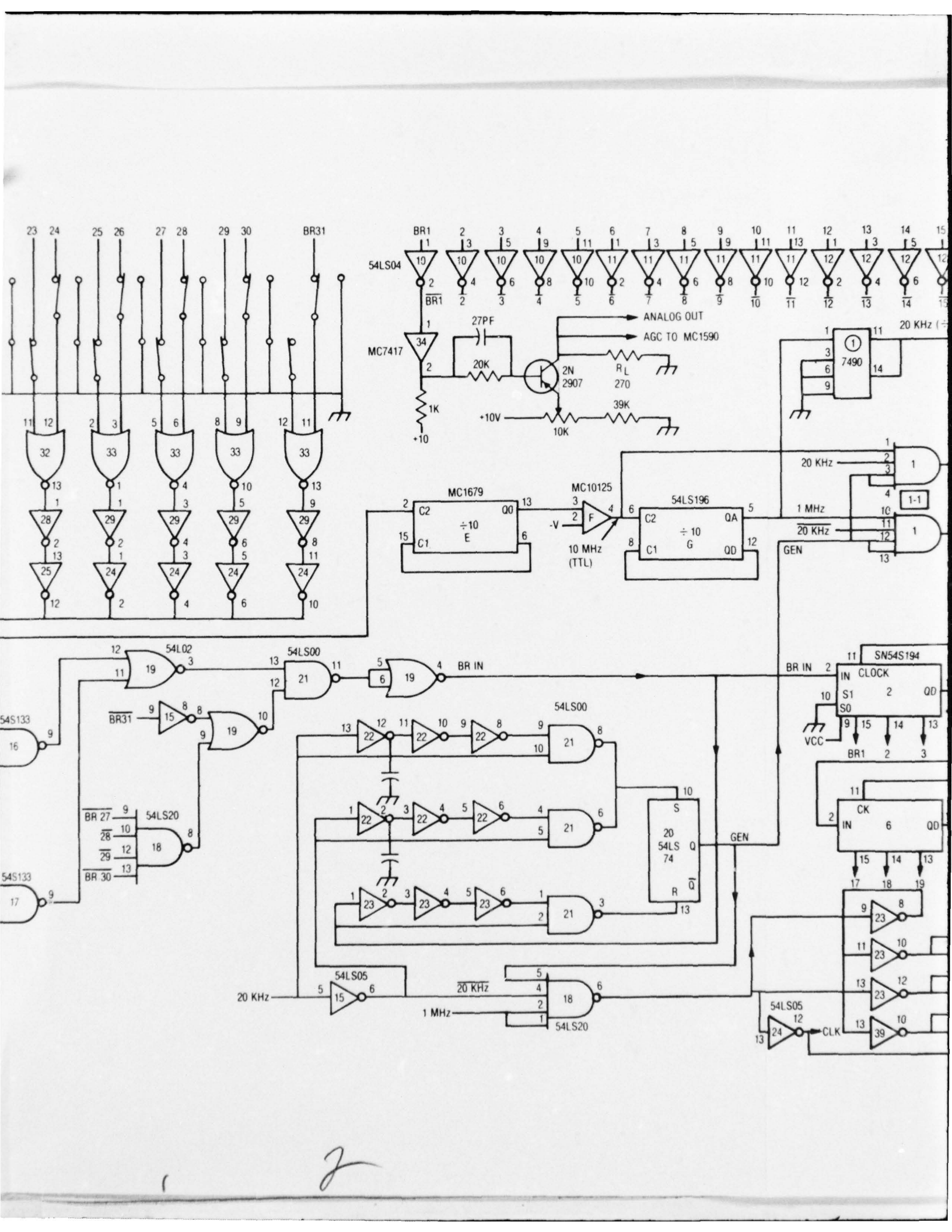
The 31-bit shift register is supplied a 1 MHz clock when the 20 kHz input goes to "0" by setting F/F-2 and enabling the 1 MHz input gate to the clock of the shift register. Now the shift register shifts through at a 1 MHz rate and produces the analog voltages that supply the input analog voltages in synchronization with the 1 MHz clocks. The analog voltages are now stored in the bucket brigade.

With reference to the timing diagram of Figure 30, during the first 3.1 μs of the 5 μs pulse, the shift register is shifting at "1" through the register at a 10 megabit rate. Immediately after the pulse, a "1" is shifted through the register in 31 μs at a rate of 1 megabit per second.

The logic functions for the tester were implemented primarily with Motorola MECL III and Shottky TTL. A more detailed schematic of the tester is shown in Figure 31. The various logic circuits and parts are indicated on the diagram.

Photographs of the assembled tester are shown in Figures 32 and 33. Figure 32 shows the parts assembly and Figure 33 the control switches, bias plugs and input-output connectors. The phase input to the shift register is controlled manually by 31 individual two-pole toggle switches. The bucket brigade voltage control is obtained by off-on switches and associated variable resistors. In the assembly and check-out of the tester it was necessary to carefully isolate the rf, dc and clock signals in order to prevent interference.


BR1 BR2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
54L02
54LS04
54LS05
+V
MC10124
D
1K
+5V
-5V
54LS05
SR INPUT
1K
VDD
AGC INPUT
+10V
100 Ω
BNC
1 Hz
IN
B
100 MHz
MC1673
B
1 μF
1K
MC1590
0.33 μF
51 Ω
BNC
RF OUT
1K
-5V
1 μF
54S133
16
54S133
17
BR1
BR 26
BR31
BR 27
BR 30
54LS


BR31
54LS04
MC7417
27PF
20K
2N
2907
R_L
270
1K
+10
+10V
10K
39K
ANALOG OUT
AGC TO MC1590
20 KHz
7490
MC1679
÷10
E
MC10125
-V
10 MHz
(TTL)
54LS196
÷ 10
G
1 MHz
GEN
54L02
54LS00
BR IN
54S133
BR31
54LS20
BR 27
BR 30
SN54S194
CLOCK
VCC
BR1
20
54LS
74
54LS05
CLK

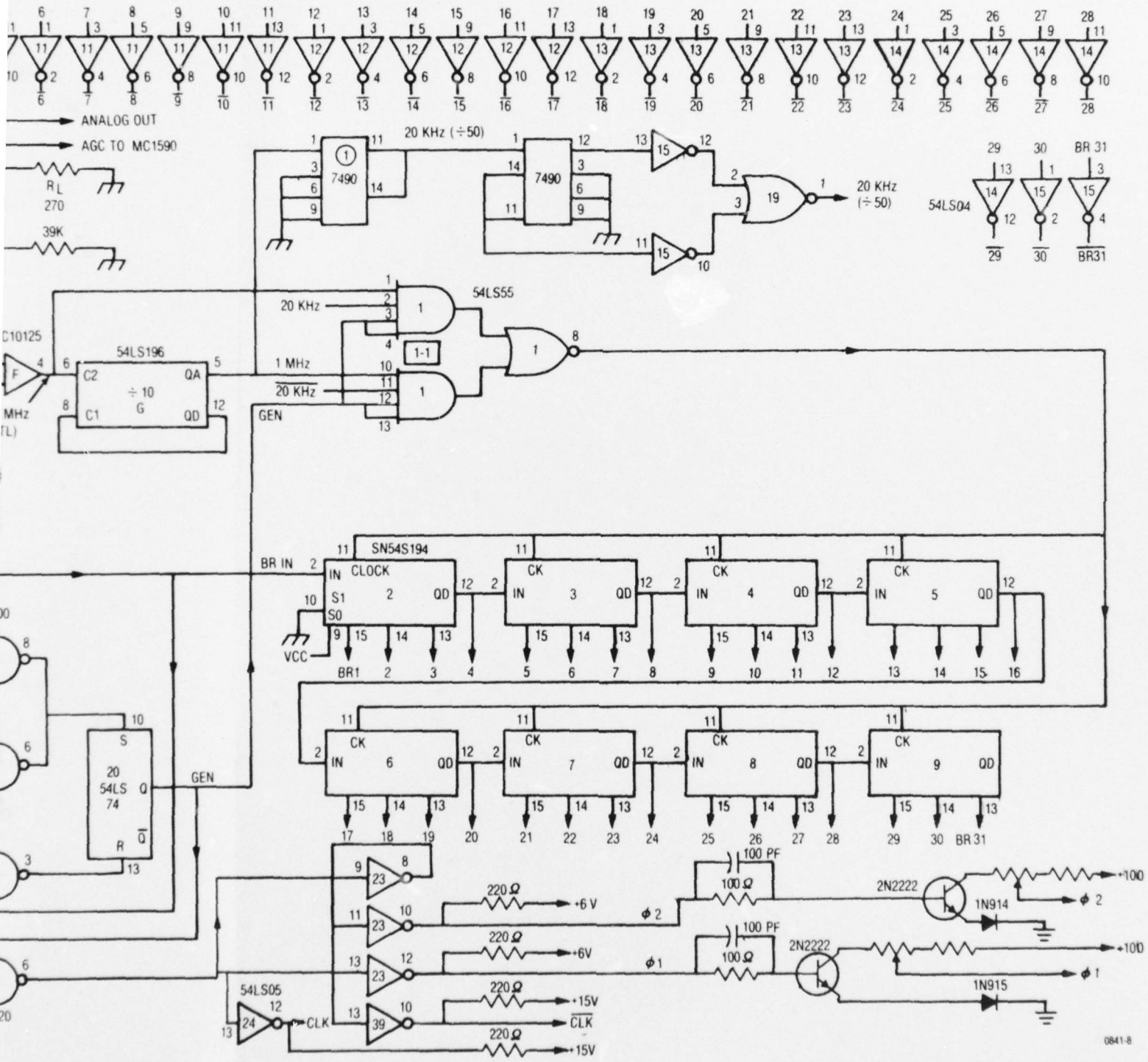


Figure 31. Detailed Schematic of the Programmable Tester

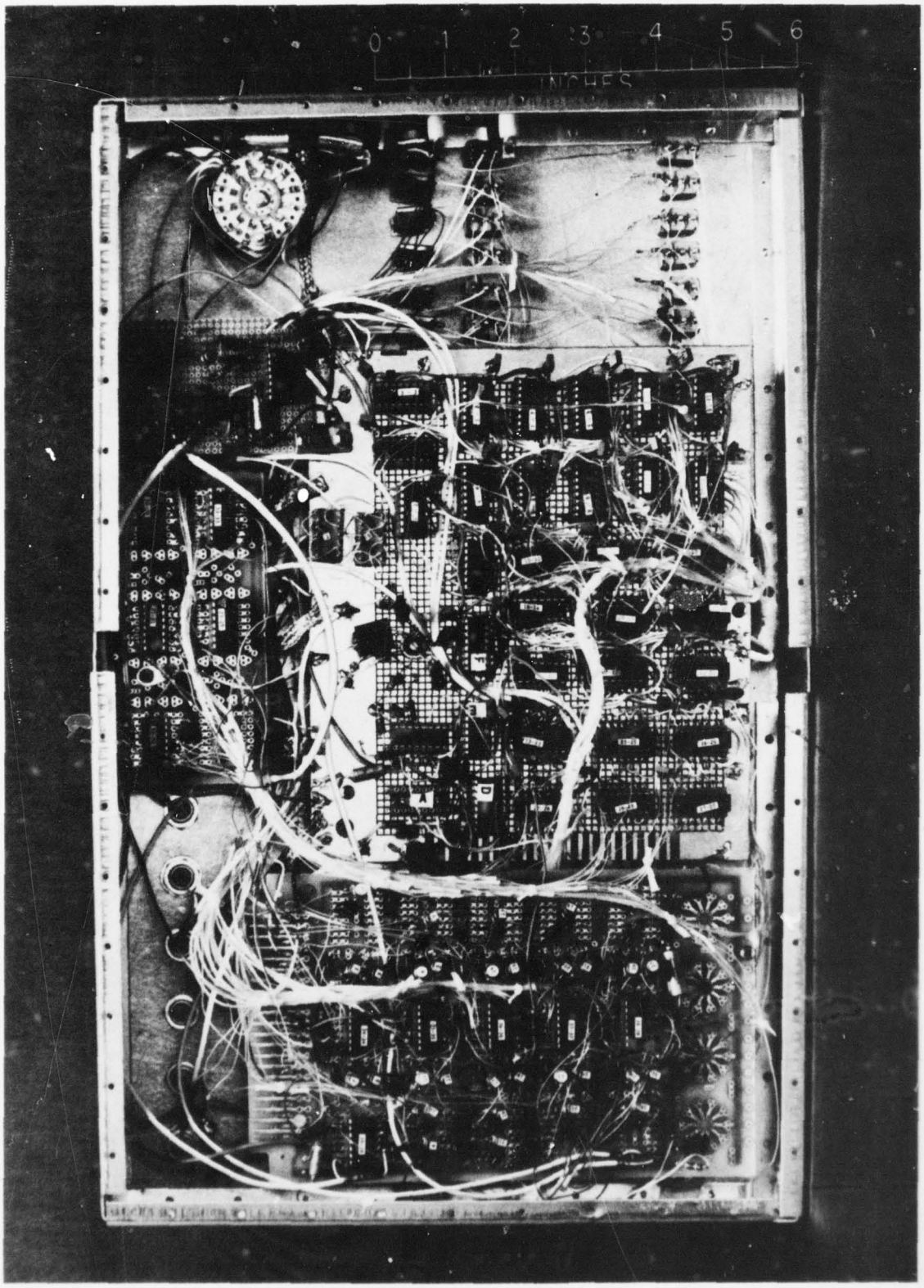


Figure 32. RF Tester - Parts Assembly

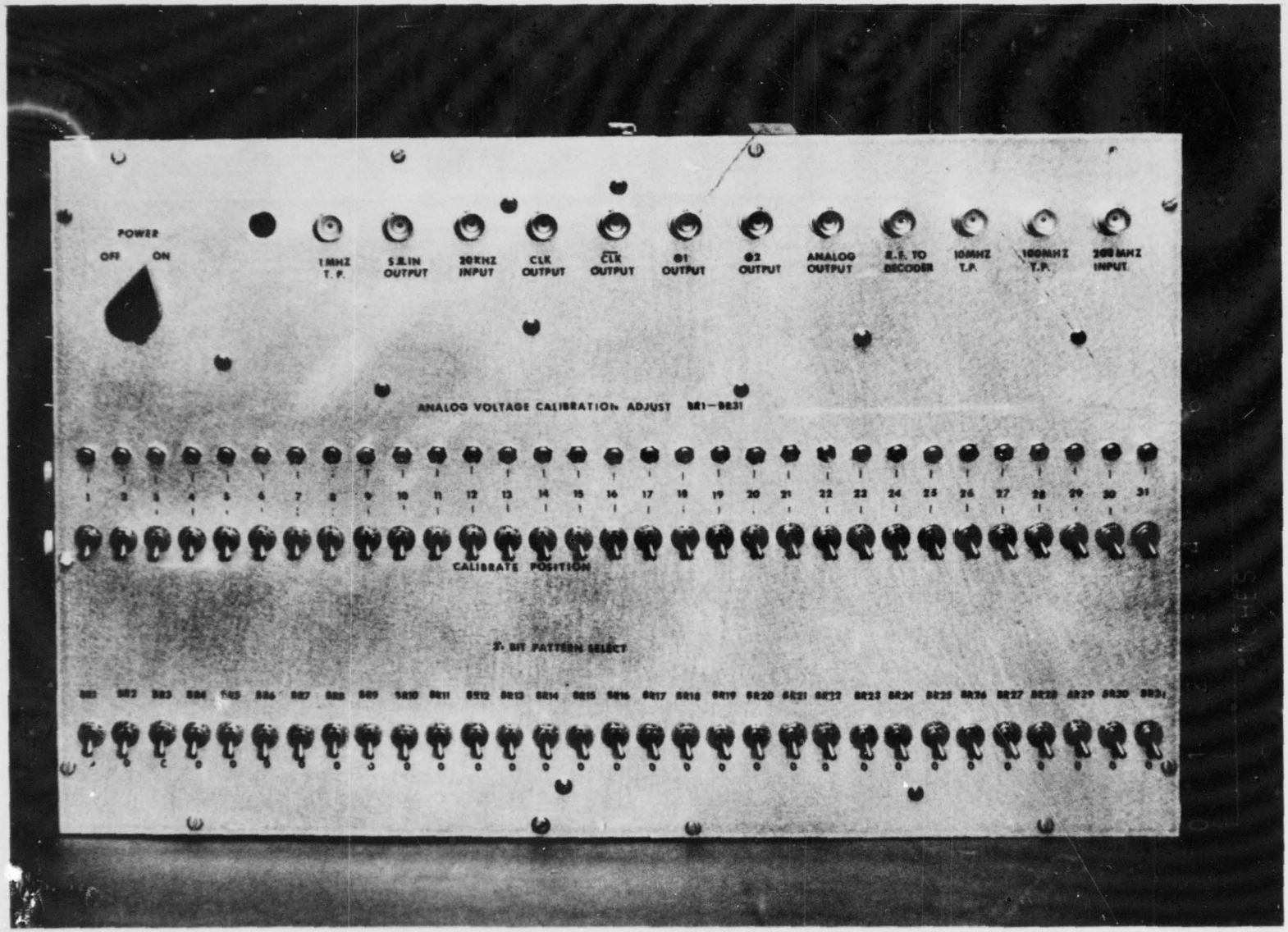


Figure 33. RF Tester - Control

SECTION VIII

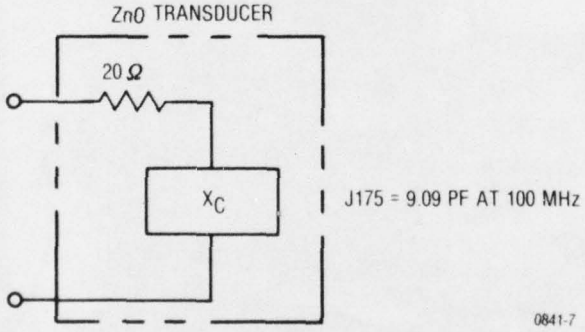
RF DEVICE TESTING

1. INTRODUCTION

The original intent was to test the full phase and amplitude programmability of the monolithic surface wave transversal filter in the correlation or decoding mode. However this was not possible due to specific problem areas. It was possible to comprehensively evaluate the three basic functional parts of the device and operate it with full logic in an encoding mode. This was done through hard-wiring and using the programmable tester with an external pulsed frequency generator. Figure 34 shows the bench assembly of test equipment used to evaluate the transversal filter and Figure 35 is a closeup of a device under full logic testing. A description of the various tests and the results follow.

2. TRANSDUCER CHARACTERIZATION

The impedance of the ZnO input transducers were first measured on an HP Network Analyzer using a polar display plug-in unit. Impedance information was taken directly from the Smith Chart plot obtained from the polar plug-in unit. The typical impedance measured at 100 MHz was 20-j175. This gives the following series equivalent network;



An unloaded Q of 8.75 is calculated. The electrical Q from the center frequency bandwidth calculation is 10. The loaded Q of the network working into a 50Ω system will be approximately 2.5.

The capacitive reactance was resonated using a series inductor consisting of a torroidal permeable core with 14 turns of #34 wire. The resulting mismatch loss was less than 0.5 dB and the 3 dB bandwidth of the impedance match was greater than 10 MHz.

RF signal testing between transducers at each end of the device helped characterize loss and bandwidth properties. The typical response of the output transducer to an input pulse of 100 ns at a frequency near 100 MHz is that shown in Figure 36. It consists of the output pulse plus trailing pulses indicative of reflections in the transmission path. The matched loss to the main pulse was approximately 40 dB under matched conditions. The first trailing pulse was only 6 dB below the main output.

Figure 37 shows a typical swept frequency response. The problem of reflection in the transmission media manifests itself as a notch in the frequency spectrum. The CW frequency loss was near

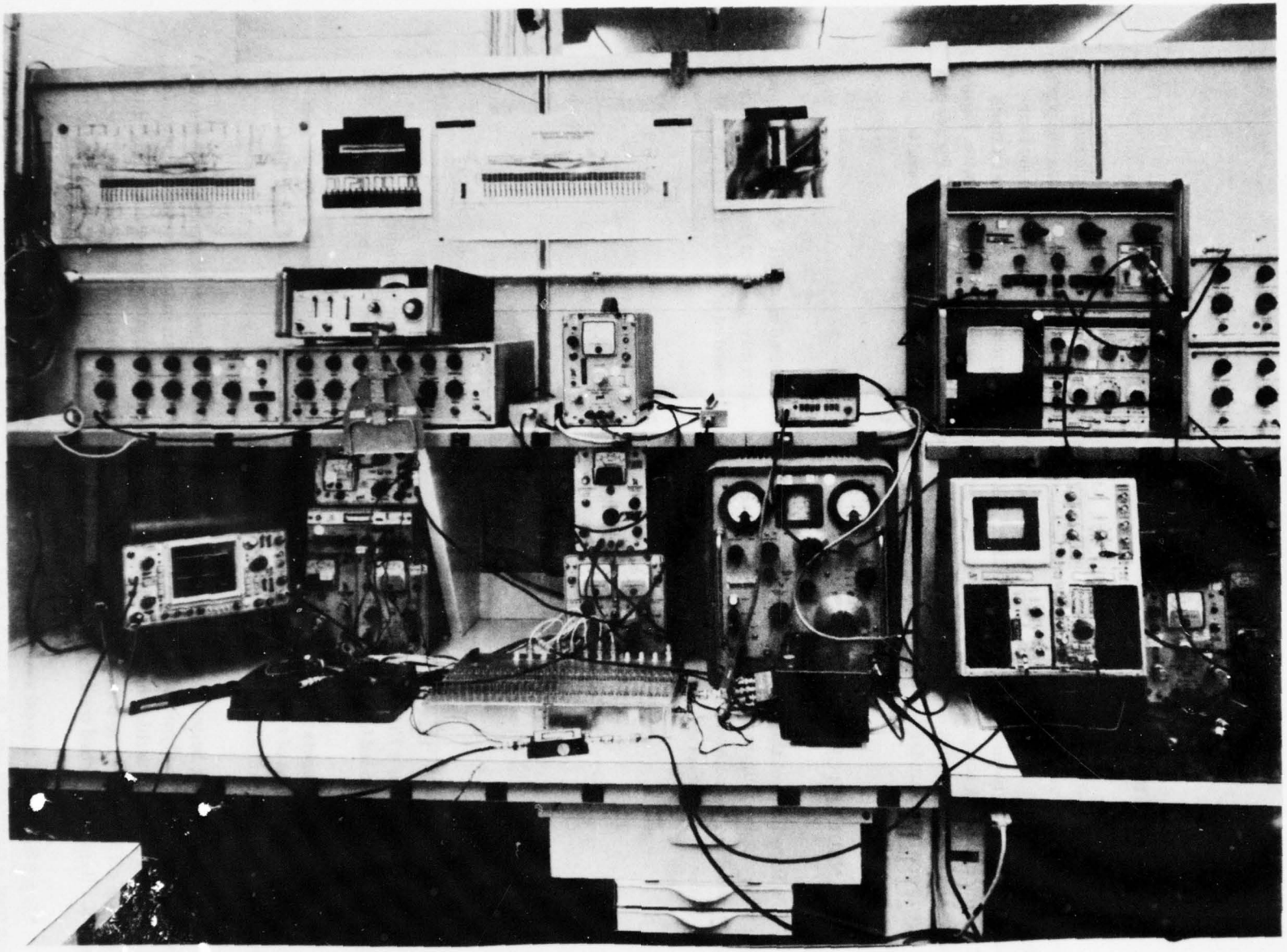


Figure 34. Test Equipment Set-Up for Evaluation of Monolithic Surface Wave Transversal Filter

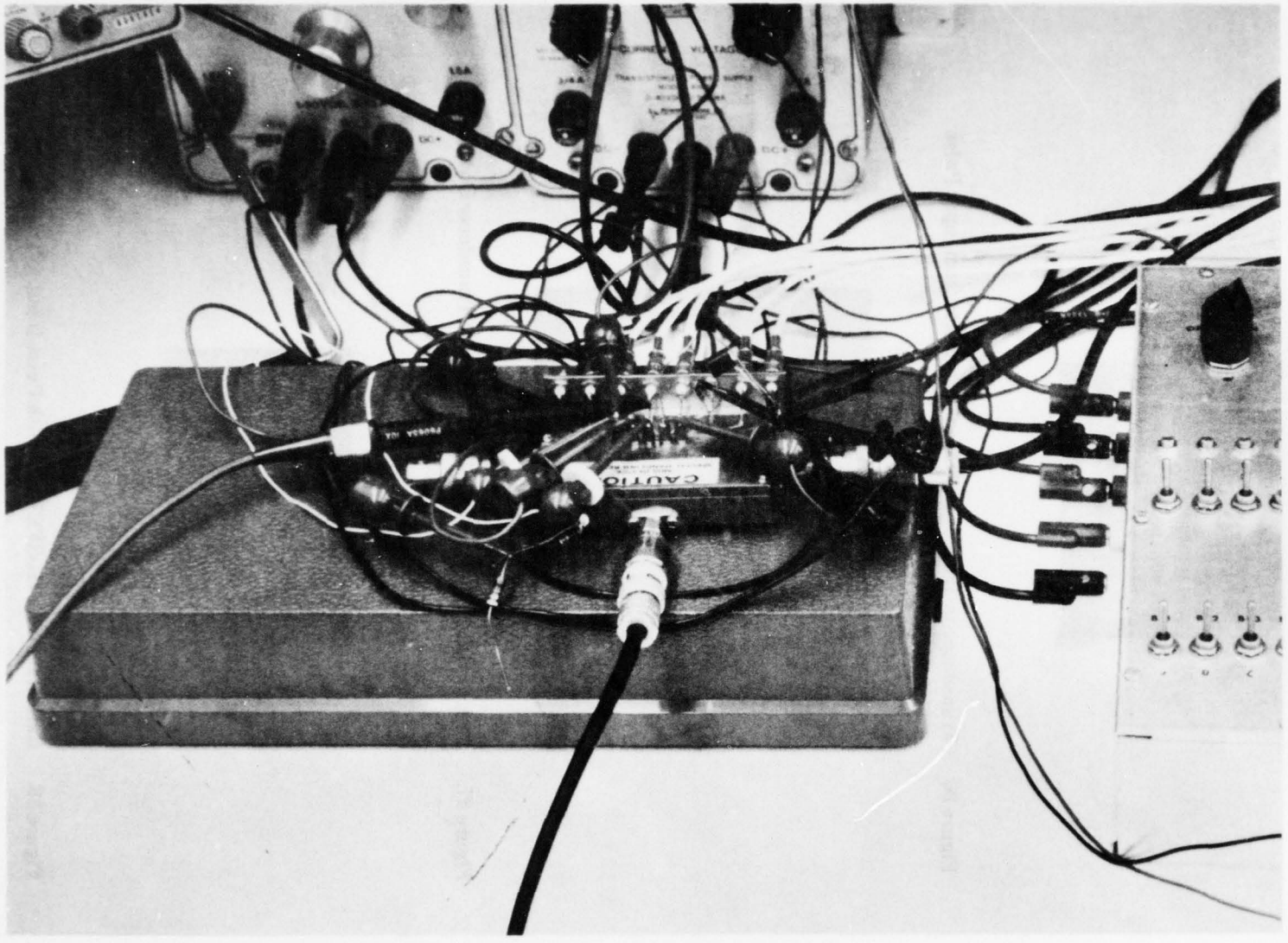


Figure 35. Surface Wave Transversal Filter Under Full Logic Testing

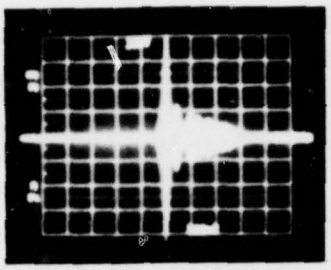


Figure 36. Transducer-to-Transducer Output Waveform from Input Pulse

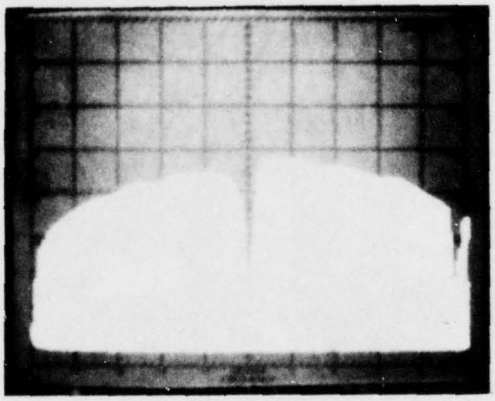


Figure 37. Swept Frequency Response of Transducer to Transducer Output

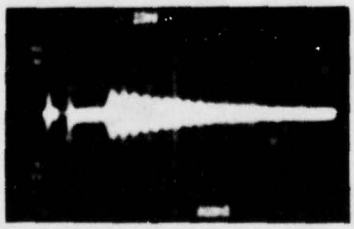


Figure 38. Reflection from MOSFET taps with Pulse Input to Transducer

35 dB and the 3 dB bandwidth for the transducers (ignoring the notch) was approximately 6 MHz. Reflection points in the spectrum were at 5 MHz intervals representing a 200 ns time equivalent to a round trip between MOSFET structures.

Pulse measurements were also made through one transducer, using it as input and output, to observe points of reflection in the transmission media. Figure 38 shows a scope photograph of such a measurement. The first reflection occurs at 1.2 μsec, (round trip position of the first MOSFET tap), and there is a decay rate of approximately 1 dB per pulse.

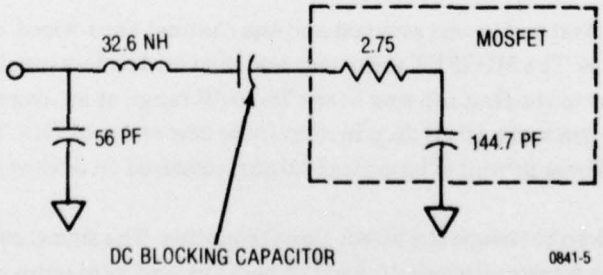
It was apparent that the MOSFET taps were reflecting part of the surface wave energy and causing attenuation of the signal. This attenuation factor was measured to be 10 dB using the MOSFET output data to be described in the next subsection. This means that the matched conversion loss for two transducers was approximately 30 dB yielding a single transducer loss of 15 dB. The 3 dB bandwidth for a single device was 9.0 MHz.

The unmatched pulsed transducer loss was also measured. This gave a corrected value of 28 dB for a single transducer.

3. MOSFET TAP CHARACTERIZATION

The untuned input impedance of the 31 tap MOSFET detector array was measured on the HP Network Analyzer with and without drain voltage applied. Because of the high capacitance of the MOSFET array, the small inductance of the wire bonds to the MOSFET drain line and the package pin causes the detector array to resonate at 100 MHz with 8 volts drain bias applied. The lead inductance makes the measurement of the input impedance of the MOSFET difficult.

The impedance measurements referenced the impedance to the outside of the package. The MOSFET impedance at 100 MHz is 2.75 $-j11$. This yields an unloaded Q of 4. The matching network used to match the detectors is shown below.



The matching network maintained a 20 MHz 3 dB bandwidth with a resulting mismatch loss of 1.7 dB.

The earliest measurements of the MOSFET tap properties were made by bypassing the bucket brigade and hardwiring the taps so that the gate voltage could be directly applied. Figure 39 shows three pairs of photographs representing output from the first, sixteenth and thirty-first tap positions of the MOSFET array in response to a pulsed 100 ns input to the transducer. The column on the left shows the pulse output from a single phase and the column on the right is a composite of the signal output at "0" and "180" phase. The losses to the taps were 74 dB, 80 dB and 85 dB respectively. This gave a loss of 11 dB across the array or approximately .35 dB per tap. The composite shows good phase reversals and equal amplitudes at the first tap with a degradation in amplitude at the sixteenth tap of approximately 2 dB and a slight phase differential. The phase differential is even more pronounced on the 31st tap with again approximately 2 dB difference in amplitude. By pulsing the transducer at the opposite end it was determined that the phase shift was due to the geometric positioning of the MOSFET taps and the amplitude difference was due to a difference in the transmission properties of the two channels. It is recalled that there is an asymmetry in the two taps due to the relative position of the gate voltage line addressing the tap nearest the drain summing lines.

The signal output from a single hard-wired MOSFET tap was measured as a function of drain current by varying the drain and gate voltages. The purpose of the test was to determine the dependence of the MOSFET output on drain current and the device saturation level. The first MOSFET tap of the array was chosen to minimize reflection effects. Figure 40 graphically depicts the results. The signal output from the MOSFET tap is normalized to 0 dB at the 5 mA drain current level and plotted as a dB increase in signal above this level as drain current increases. Four different drain-to-source voltage levels were selected and held constant as the gate-to-source voltage was varied to achieve a particular drain current level. Theoretically the tap output should increase as the square of the drain current. As seen from the graph, this relationship holds reasonably well to drain currents near 30 mA. A further increase in drain current shows a deviation from square law and eventual saturation of the output.

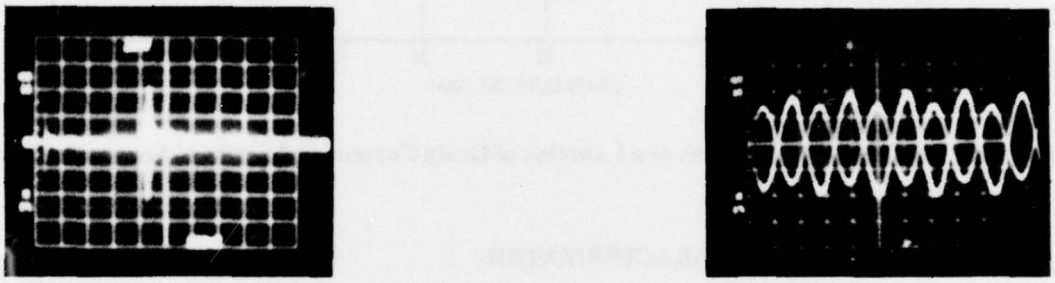
Over the range of drain currents from 5 mA to 40 mA the absolute value of loss for an individual tap decreased from 82 dB to 66 dB. The single transducer loss was calculated from pulse transmission measurements to be approximately 15 dB. Subtracting out this loss plus 3 dB due to channel splitting, the MOSFET conversion efficiency was in the range of 64 dB at the 5 mA level and 48 dB at the 40 mA level. Because the tuning was not adjusted to optimize output for a single tap, these loss levels are higher than those calculated for a single tap when activating the entire array.

A device from the first wafer was selected and one channel hard-wired with the gate voltage applied to the entire 31 taps. The MOSFET array was matched for low loss consistent with the required bandwidth. The loss to the first tap was in the 78-80 dB range at an average current of 15 mA per tap. The output waveform had a 10 dB drop in amplitude across the 31 bits. The signal feedthrough level was 72 dB. These proved to be typical values measured on devices from the first wafer.

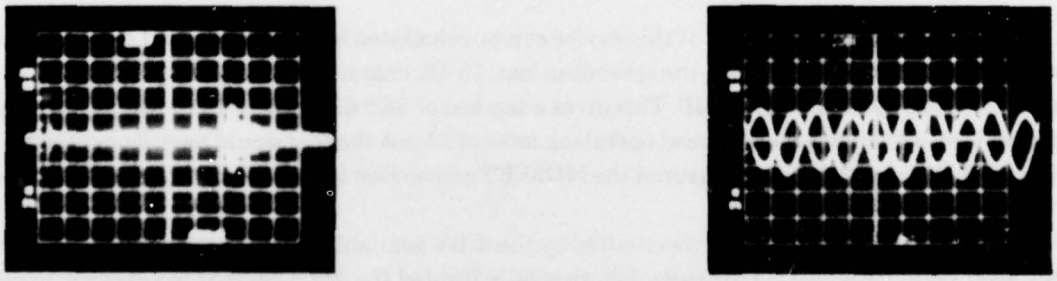
Measures were taken to reduce the direct signal coupling. The signal coupling was reduced to as low as the 90 dB level by improved grounding of the package and by placing a metal shield in the package between the transducer and the MOSFET array. Without shielding the signal feedthrough level could be brought to 86 dB. The results show that signal feedthrough is not an inherent problem in this type of device. The ground plane beneath the transducer structure is felt to have made a major contribution to the improvement in the signal feedthrough level.

TAP NO. 1

TAP NO. 16



TAP NO. 31



0841-4

Figure 39. Single MOSFET Tap Outputs from First, Sixteenth and Thirty-First Taps

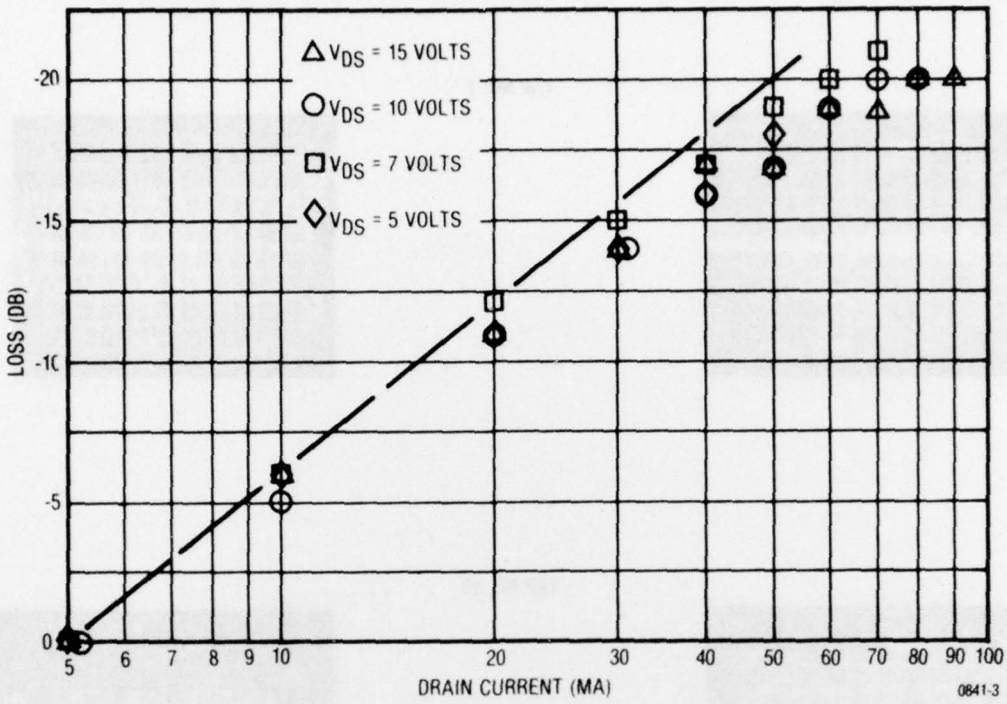


Figure 40. MOSFET Tap Output as a Function of Drain Current and Drain-to-Source Voltage

4. FULL OPERATIONAL CHARACTERIZATION

Devices from the first and second wafer were operated in an encode mode using shift register and bucket brigade circuitry. Figure 41 shows the output signal from a wafer 2 device with a single channel turned on. The device was operating at 98 MHz with a loss to the first tap of 76 dB, a 10 dB signal droop and an 83 dB feedthrough level. The drain current was approximately 7.4 mA per tap. The dip in the signal is due to a malfunction of one of the bucket brigade switches on the tester.

The MOSFET tap efficiency of this device can be calculated by subtracting out the transducer loss which was measured at 17.5 dB, the spreading loss, 15 dB, channel splitting loss, 3.3 dB, and a mismatch loss of approximately 1.7 dB. This gives a tap loss of 38.5 dB at the 7.4 mA level. If the tap could have been driven to a more typical operating level of 15 mA the loss would have decreased by another 6 dB. Of several devices measured the MOSFET conversion loss was in the 35 to 40 dB region.

The gate voltage to the taps was limited by the drive available from the bucket brigade. This voltage level varied from device to device, but generally limited the drain current to values of 10 mA or below. This was due to the change in threshold voltage with substrate bias, "body effect".

The bucket brigade could be used to change tap amplitude effectively. Individual taps could be turned on and off and their amplitude varied continuously within a 10 dB dynamic range. Figure 42 shows a leveling of the output waveform by adjusting individual tap amplitude levels.

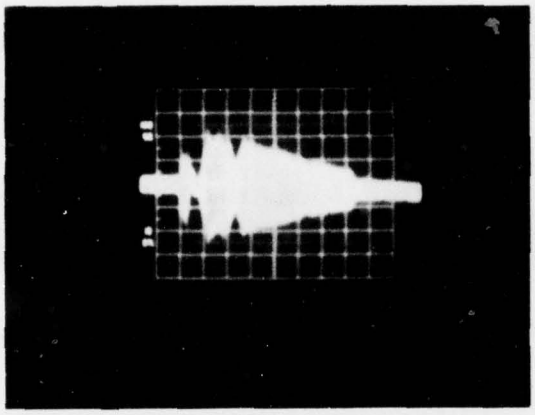
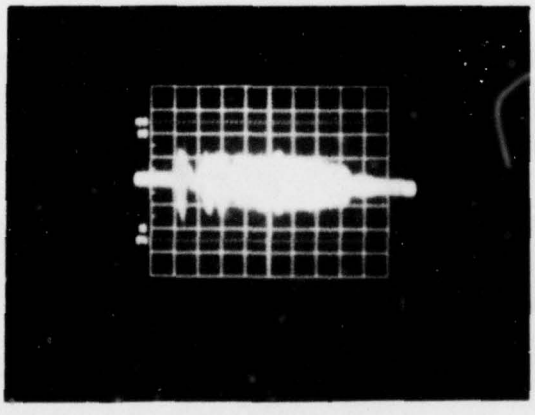


Figure 41. Signal Output From Single Channel MOSFET Tap Array



0841-2

Figure 42. Signal Output from Single Channel MOSFET Tap Array with Amplitudes Leveled by the Bucket Brigade

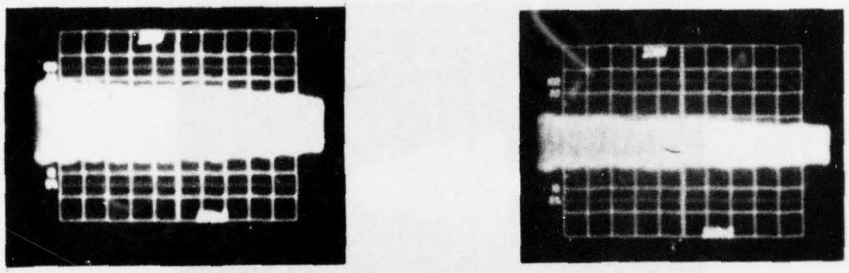


Figure 43. Phase Reversal of a Single Channel of MOSFET Taps

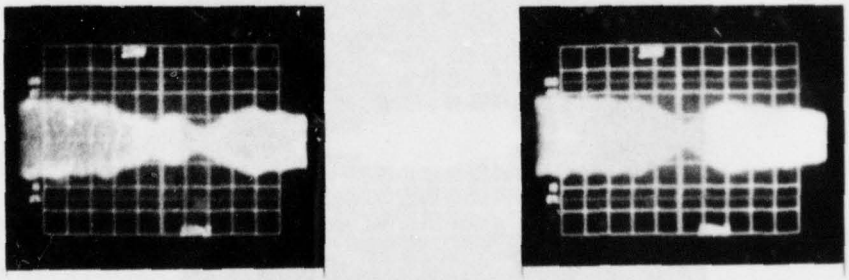


Figure 44. Tap Phasing Switched by Shift Register

The shift register provided control of the tap phase. Figure 43 shows the outline of a section of the code in the two different phase conditions. The purity of the phase reversal of an individual tap in relation to immediately adjacent taps was not as good as anticipated. Figure 44 shows the amplitude degradation for a single tap phase switched and for three adjacent taps switched. The problem was traced to off-on ratios in the shift register which is correctable through design changes. This phasing problem was the primary one preventing the measurement of correlation properties since there would be amplitude degradation of the signal as evidenced in Figure 44.

Operation of the transversal filter with full logic implementation showed that the concept is a viable one and it is only necessary to correct specific limitations in order to realize a functional device which can be implemented in communication equipment.

SECTION IX

PERFORMANCE ANALYSIS

1. PERFORMANCE ANALYSIS

a. Thin Film ZnO Transducers

The thin film zinc oxide transducers evaluated had matched insertion loss values in the 15 dB region with a 3 dB bandwidth of 9 MHz. The k^2 coupling factor calculated from the electrical impedance measurements was in the range 0.6 to 0.7%. The coupling factor from untuned loss measurements was calculated to be in the range of 0.5 to 0.6%. This compares to a theoretical coupling factor of 0.8%.

The coupling factor was found to be fairly uniform over an entire wafer. An average coupling factor within 75% of theoretical indicates good but not exceptional film quality. The sputtered ZnO film technology is capable of coupling factors within 90% of theoretical which would lower the tuned insertion loss and improve overall device performance.

b. MOSFET Detector Taps

The insertion loss at an individual MOSFET tap under typical drain current operating conditions was in the 35 to 40 dB range. Using the measured channel conductance values and a bias reduced gauge factor, a tap efficiency of 30 to 35 dB would be predicted. This is in reasonable agreement with the measured value but does indicate the possibility of additional dissipative loss mechanisms. It is felt that the NMOS technology is capable of bringing the conversion efficiency per tap to the 30 dB level.

The design of a high conductivity plane at the silicon-oxide boundary under the transducer electrodes was effective in reducing direct signal feedthrough paths within the silicon. Good grounding was also a key to signal isolation. By obtaining isolation as high as 90 dB there does not appear to be any inherent problem of direct signal coupling associated with this technology.

The problem of signal droop focused on the physical structuring of the MOSFET taps. There were discontinuity levels as high as 2.0 microns or approximately .04 wavelengths. An SEM photograph of the topography is shown in Figure 45. A reflection coefficient of .056 was calculated from measurements made of the signal level difference between adjacent taps and the transducer and first tap. This permitted a quantitative empirical relationship to be deduced relating reflectivity to thickness to wavelength ratio. The relation was that the reflectivity of an individual tap equaled $1.34\ h/\lambda$.

The foregoing reflectivity factor can be used to determine a maximum structural discontinuity level which can be tolerated if the signal droop is to be less than a given value. For example, to maintain less than 2 dB droop across 31 taps requires that the structural discontinuities be less than 8000 Å. This is better than a 50 percent reduction in the present structural size. Such a reduction appears possible using a silicon gate technology and/or buried layers.

The main dc power required for device operation is that supplied the MOSFET taps. There are approximately 3.0 watts required to operate the 31 taps at a good efficiency level. This is 100 milliwatts per bit of tap information.

Tap-to-tap amplitude uniformity and phase purity was very good between adjacent taps and taps of opposite phase neglecting the reflection problem. There was a minor placement error in tap position evident from the electrical measurements at the load end of the device. This was most likely a masking error and easily correctable. There was very good tap-to-tap signal isolation.

c. BBD-DSR Control Circuitry

The control circuitry performed the functions of tap phase and amplitude control. The performance of the bucket brigade and digital static shift register were evaluated as separate circuit elements and in conjunction with their ability to control the taps. As a separate element the digital shift register worked as designed with rates to 10 MHz. The bucket performed well but limited at voltage level inputs above 4.5 volts. This was the "body effect" mentioned previously.

There was a problem with the phasing of individual taps. This was traced to off-on ratios in the shift register circuitry and is design correctable.

The bucket brigade limitation kept the range of amplitude change at taps to 10 dB. The tap amplitude was continuously variable over this range.

The dc power required to operate the shift register was less than 1.0 watt. The bucket brigade operated at less than 0.1 watt.

d. Comparison with Previous Device Development

Table 7 compares the previously developed ROM controlled filter with the BBD-DSR controlled filter. In the zinc oxide transducer area the thick versus thin film technologies gave similar results. The ease of fabrication favors the thin film approach in future developments.

The NMOS detector taps had a somewhat better conversion efficiency and saturation level. Based on these results the NMOS technology for the taps is favored.

The device performance was similar. The main exceptions were the improved feedthrough and the slightly higher signal droop.

The control circuitry was different for the two devices and therefore not amenable to direct comparison. Obviously the BBD-DSR circuit had greater programming flexibility but a lower speed. The yield was higher for the NMOS Technology.

The factors compared favor NMOS Technology. It will be necessary to gain better control over the threshold voltage change if NMOS is used in future developments.

TABLE 7. COMPARISON ROM AND BBD DSR PROGRAMMABLE FILTERS

PARAMETER	TECHNOLOGY	
ZnO Transducer	Thick Film	Thin Film
Matched Loss	15 dB	15 dB
Bandwidth	9.5 MHz	9 MHz
K^2 Coupling	.74%	0.6%
MOSFET Tap	PMOS	NMOS
Loss/Tap	40 dB	35-40 dB
Gate Threshold	2-2.5V	1.0-1.25V
Drain Voltage	6-8V	8-10V
Tap Current	10-13 mA	8-16 mA
Saturation	>20 mA	>30 mA
Power/Tap	60-100 mW	64-160 mW
Device Parameters	ROM	BBD DSR
Impulse Loss	78-80 dB	75-80 dB
Loss to Peak	44 dB	Not Determined
Peak to Side Lobe	12 dB	Not Determined
Feed Through	70 dB	80-90 dB
Signal to Noise	20 dB	20 dB
Signal Droop	8 dB	10 dB
Power	3.2 W	3.5 W
Control Circuitry	ROM	BBD DSR
Code	Fixed	Arbitrary

TABLE 7. COMPARISON ROM AND BBD DSR PROGRAMMABLE FILTERS (CONTD)

PARAMETER	TECHNOLOGY	
Speed	3 μs	50 μs
Phase Control	Good	Good
Amplitude Control	None	~10 dB
YIELD	20%	40-50%

2. MANUFACTURABILITY

There are no major problem areas related to manufacturing the surface wave transversal filter in quantity. It was necessary to make some processing adjustments during circuit development under the program. Standard semiconductor processes and fabrication techniques are used throughout.

The yield of good devices was exceptionally high for such a large scale integrated circuit under development for the first time. The yield was in the 40 to 50% range which was substantially higher than the previous device development.

A cost per device may be estimated based upon this kind of yield in a manufacturing environment. Assuming a 1000 device development, the cost per wafer for lot processing is estimated to be $150. The zinc oxide processing step adds an additional $50 bringing wafer cost to $200. At an anticipated yield of 20 good devices per wafer, the die cost is $10. The cost of dc electrical test, visual inspect and wafer dice would add approximately $6.50. The cost of substrate and package is $12.50. The assembly and final test would be $14.00 per device. The total estimated cost per device is $43.00. This estimated price level is extremely attractive considering the functions performed.

SECTION X

CONCLUSIONS

A monolithic surface acoustic wave transversal filter with tap phase and amplitude control was developed on silicon using piezoelectric film transducer and semiconductor MOSFET technologies. This development represented a significant step toward the realization of a versatile signal processing chip for use in spread spectrum communications. To duplicate the functional capabilities of this small integrated circuit chip by lumped or hybrid circuit techniques would require a considerably more complex arrangement of electronic parts with increased volume and weight.

The fact that standard semiconductor process and fabrication techniques have been used throughout means that such transversal filter chips can be reliably produced in quantities at low cost. The simplicity of device structure and the versatility of process function afforded by the integration of SAW and silicon technologies can easily be recognized by the developments under this program.

Additional refinement of certain aspects of the technology is required to realize its full operational potential. The MOSFET detector tap geometry must have a lower topographical profile to minimize acoustic relections. Ways to improve detector conversion efficiency should be given additional consideration. The control circuitry addressing the detector taps should be designed for a higher speed of operation. The control circuit logic should interface with external logic in the most efficient manner. Improving the transducer efficiency and extending the bandwidth capability will result in an overall better device.

The technology which has been developed through the design, fabrication and testing of the monolithic surface wave transversal filter is considered to have the following implications: 1) The monolithic SAW-silicon device concept has tremendous potential for electronic signal processing. 2) There is additional basic development which is required before its full potential is realized. And, 3) present technology is adequate for the realization of that potential if engineering and scientific talent is dedicated to the task.

SECTION XI

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